

Compal Confidential

G400/G500 UMA M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

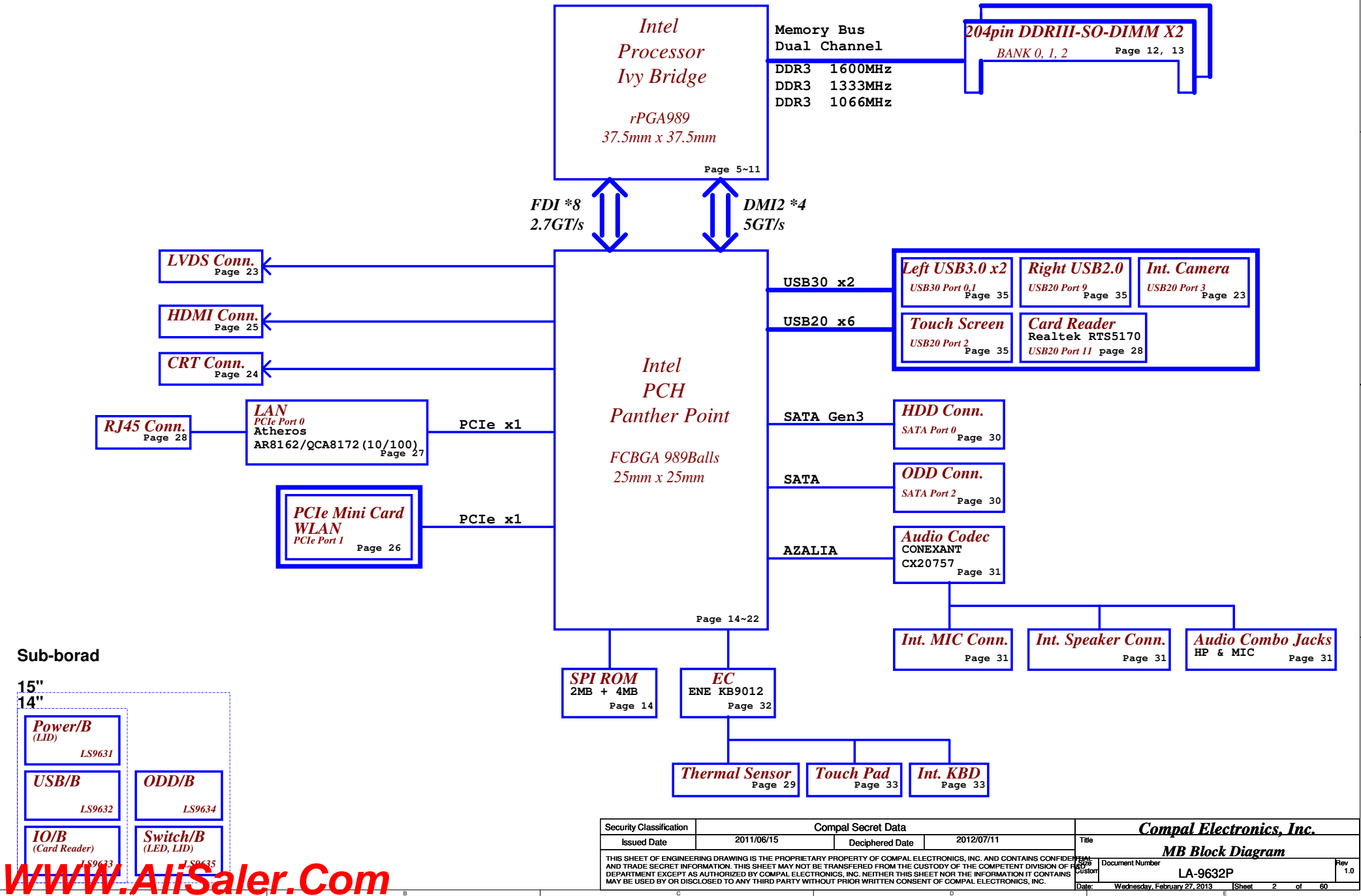
2013-02-27

LA-9632P

REV: 1.0

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Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	Cover Page	
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Chief River



Voltage Rails

power plane	+B	+5VALW	+1.5V	+5VS
				+3VS
State		+3VALW		+1.5VS
				+V1.05S_VCCP
				+VCC_CORE
				+VGA_CORE
				+VCC_GFXCORE_AXG
				+1.8VS
				+0.75VS
				+1.05VS
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

EC SM Bus1 address

Device	Address
Smart Battery	0001 011x

EC SM Bus2 address

Device	Address
Thermal Sensor	0100 1100

PCH SM Bus address

Device	Address
DDR_JDIMM1	1010 000x A0h
DDR_JDIMM2	1010 010x A4h

AMD-GPU SM Bus address

Device	Address
Internal thermal sensor	0100 0001 41h

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN	Thermal Sensor	PCH
SMB_EC_CK1	KB9012	✗	✓	✗	✗	✗	✗	✗
SMB_EC_DA1	+3VALW		+3VALW					
SMB_EC_CK2	KB9012	✓	✗	✗	✗	✗	✓	✓
SMB_EC_DA2	+3VS	+3VGS					+3VS	+3VALW
PCH_SMBCLK	PCH	✗	✗	✗	✓	✓	✗	✗
PCH_SMBDATA	+3VALW				+3VS	+3VS		
PCH_SML0CLK	PCH	✗	✗	✗	✗	✗	✗	✗
PCH_SML0DATA	+3VALW							
SML1CLK	PCH	✓	✗	✓	✗	✗	✓	✗
SML1DATA	+3VALW	+3VGS		✓			+3VS	

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Vcc	3.3V
R694	100K +/- 1%
Board ID	R695
0	0
1	12K +/- 1%
2	15K +/- 1%
3	20K +/- 1%

Board ID / SKU ID Table for AD channel

Board ID	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD	
0	0 V	0 V	0 V	0x00 - 0x0B	MP
1	0.347V	0.354V	0.360V	0x0C - 0x1C	PVT
2	0.423V	0.430V	0.438V	0x1D - 0x26	DVT
3	0.541V	0.550V	0.559V	0x27 - 0x30	EVT

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1	UHCI0	0	USB Port (Left Side) USB3.0
		1	USB Port (Left Side) USB3.0
	UHCI1	2	Touch Screen
		3	Camera
	UHCI2	4	
		5	
	UHCI3	6	
EHCI2		7	
	UHCI4	8	
		9	USB Port (Right Side USB-BD)
	UHCI5	10	Mini Card(WLAN)
		11	Card Reader
	UHCI6	12	
		13	

BOM Structure Table

Item	BOM Structure
VIWGP (14")	14@
VIWGR (15")	15@
HDMI Logo	45@
LAN 10/100	8162@
LAN 10/100	8172@
LAN Switch mode	SWR@
LAN LDO Mode	LDO@
LAN Gas tube	GAS@
Camera	CMOS@
HDMI	HDMI@
PCH is HM76	HM76@
PCH is HM70	HM70@
PCH is NM70	NM70@
VGA is Mars XT	Mars@
VGA is Sun Pro	Sun@
For VGA	PX@
For VRAM and Strap	X76@
For UMA Strap	UMA@
Microphone	MIC@
Touch Screen	TS@
Connector	ME@
Board ID for EVT	EVT@
Board ID for DVT	DVT@
Board ID for PVT	PVT@
For USB2.0 (All PCH)	USB2@
For USB3.0 (HM76, HM70)	USB3@
For share ROM	SROM@
For non-share ROM	NOSROM@

D

1

C

1

B

1

A

1

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						Custom	LA-9632P		
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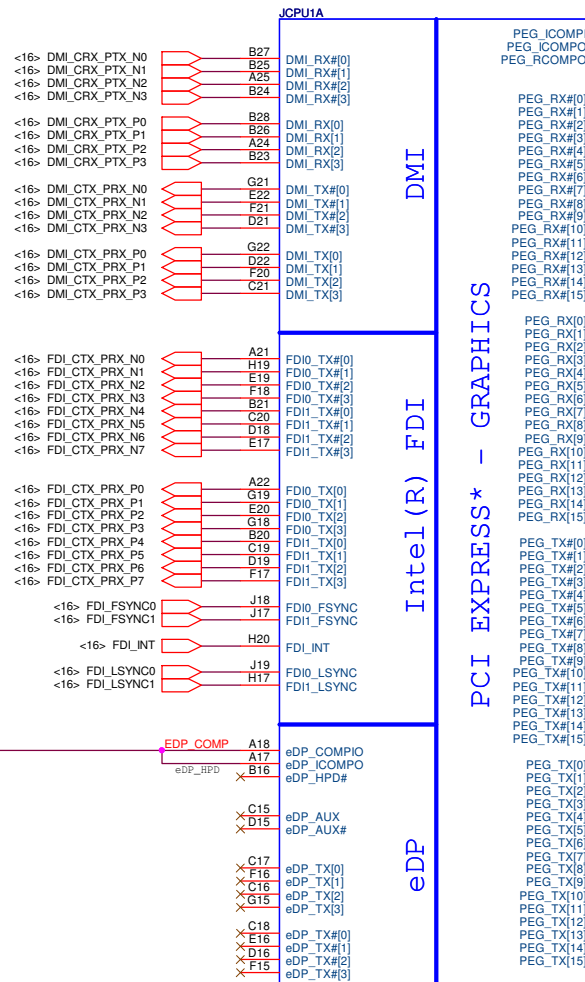
14" UMA PCB_LA9632P
DA6000WP000
PCB 0Y0 LA-9632P REV0 M/B UMA 3



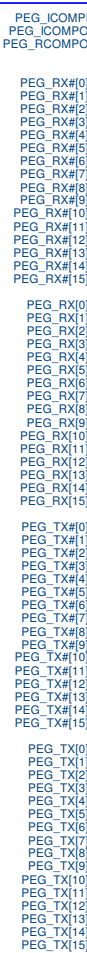
15" UMA PCB_LA9632P
DA6000WP100
PCB 0Y0 LA-9632P REV0 M/B UMA 5

PEG_ICOMPI and RCOMPO signals should be
shorted and routed
with - max length = 500 mils - typical
impedance = 43 mohms
PEG_ICOMPO signals should be routed with -
max length = 500 mils
- typical impedance = 14.5 mohms

+V1.05S_VCCP
R1
24.9_0402_1%



PCI EXPRESS* - GRAPHICS



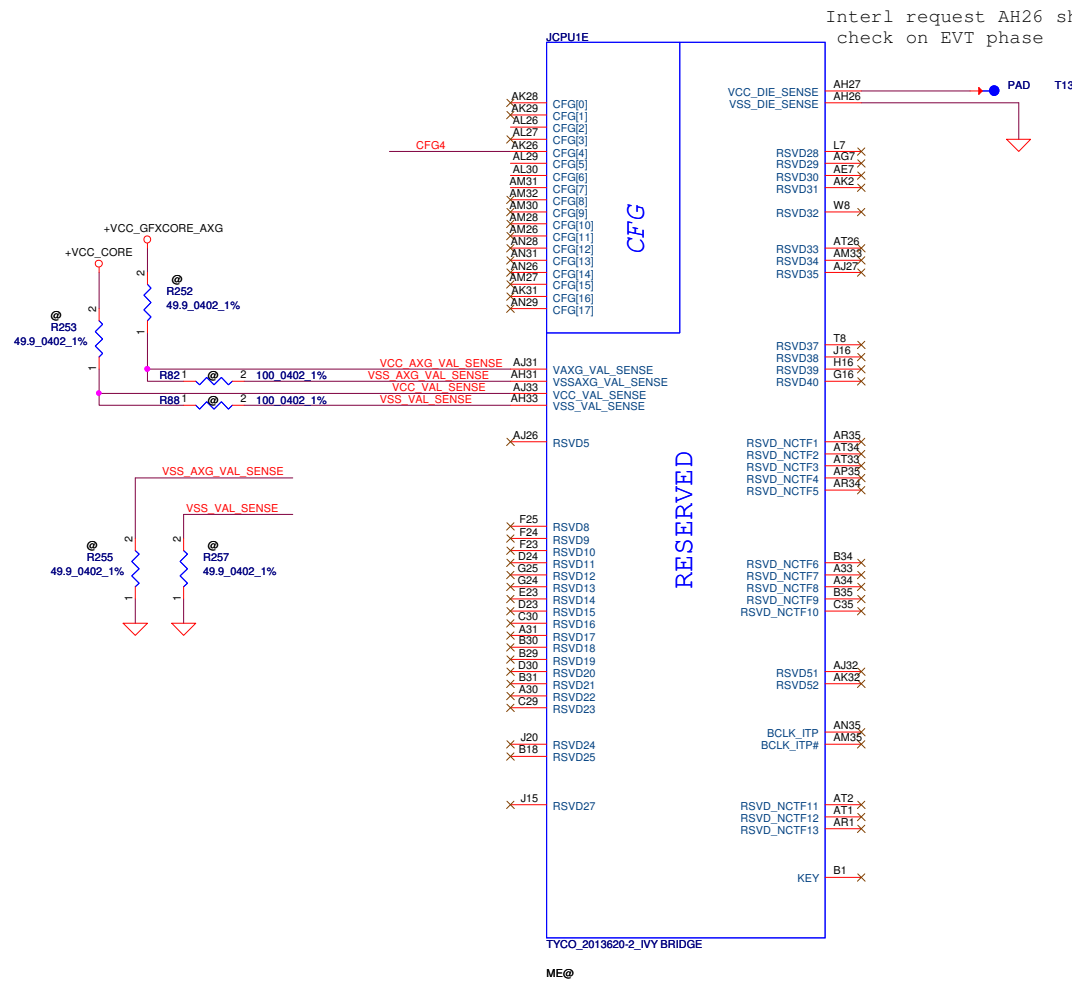
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed

eDP_COMPIO and ICOMPO signals
should be shorted near balls
and routed with typical
impedance <25 mohms

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CFG Straps for Processor

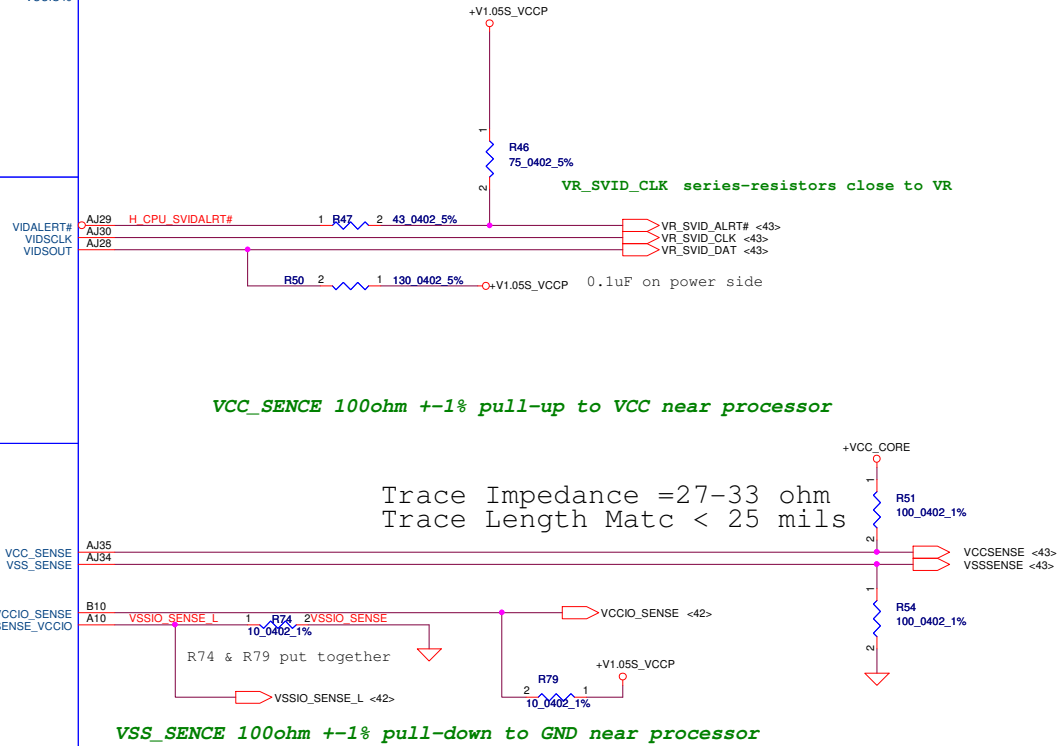
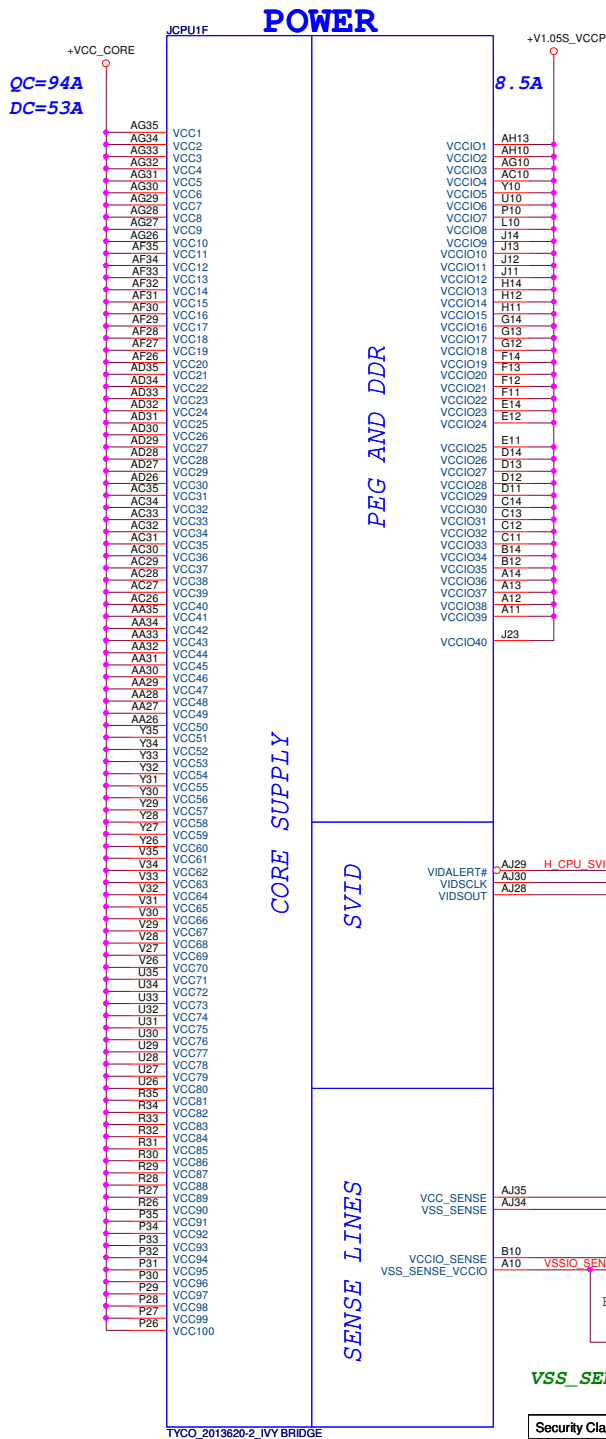


PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed

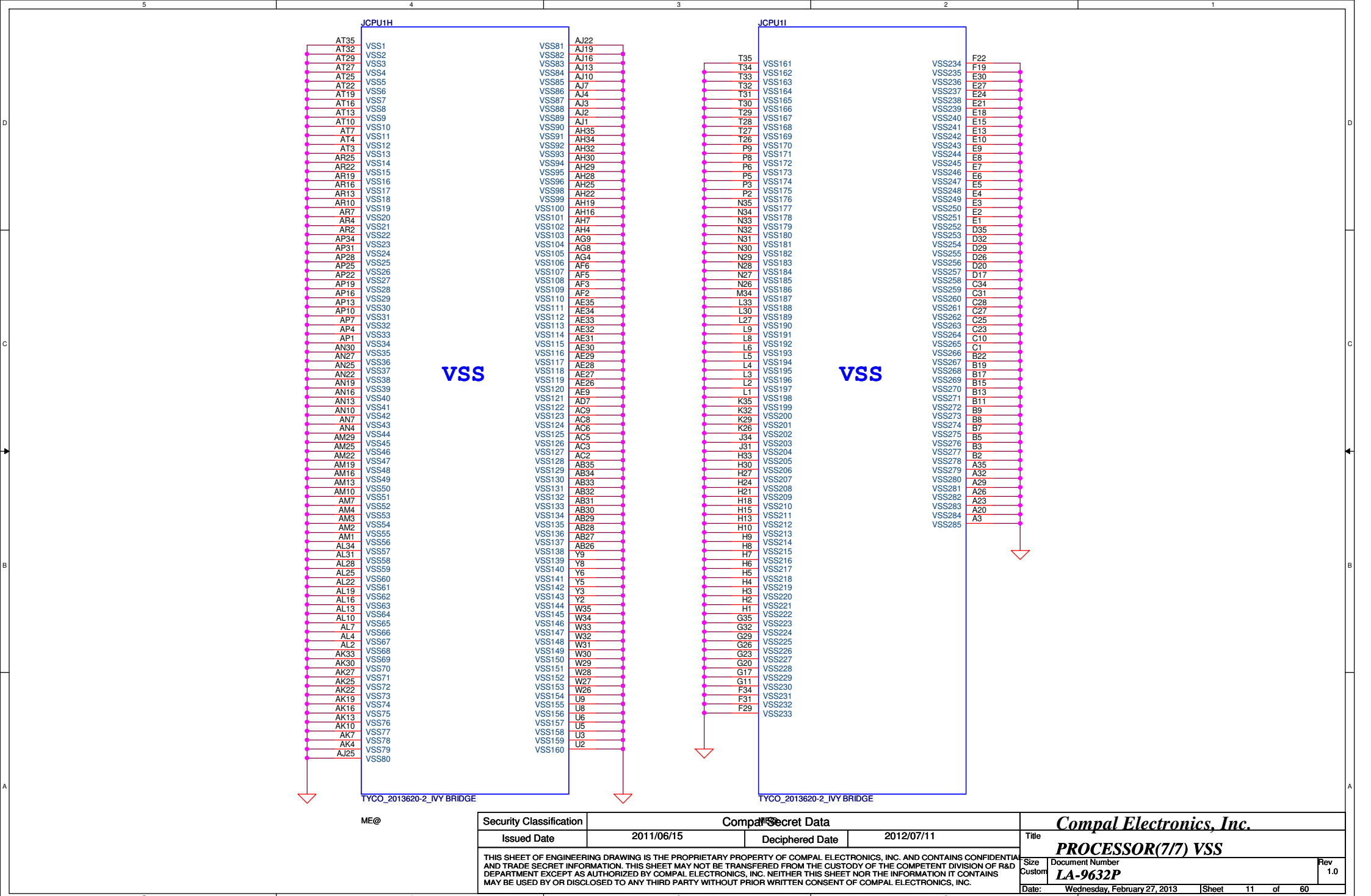
Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled * 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

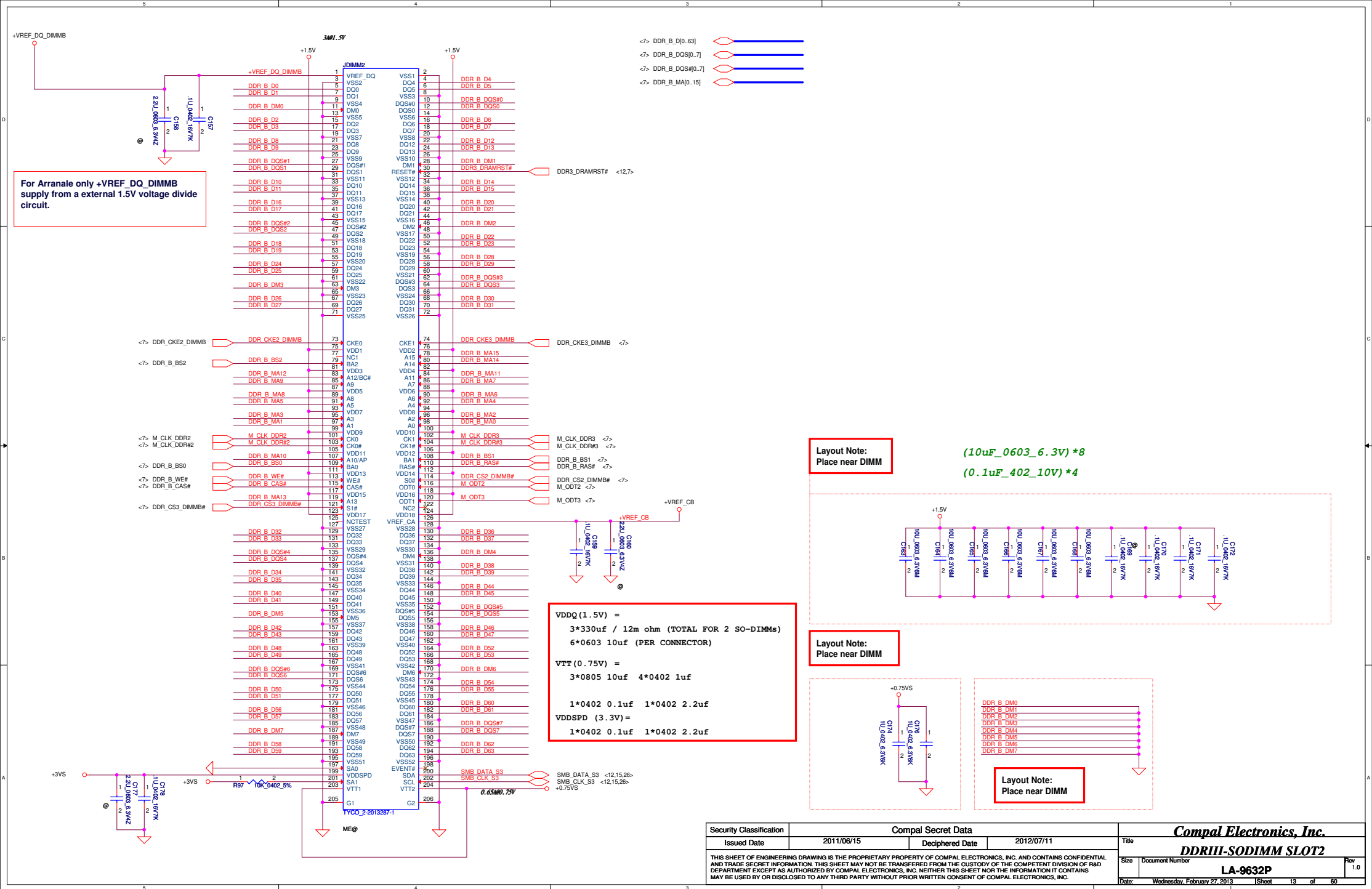
PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

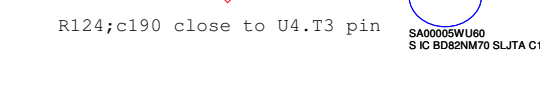
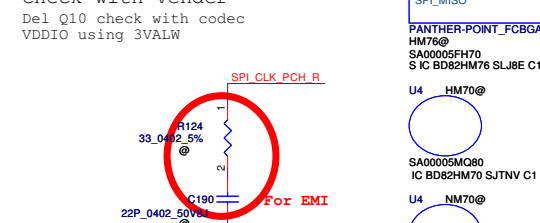
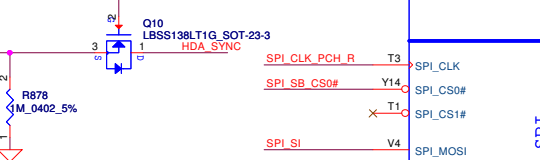
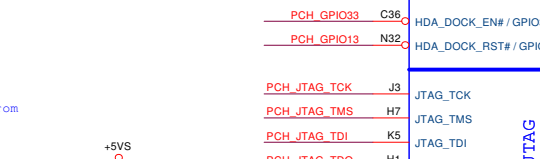
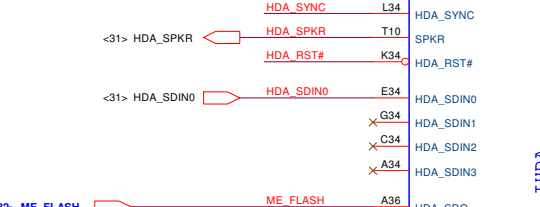
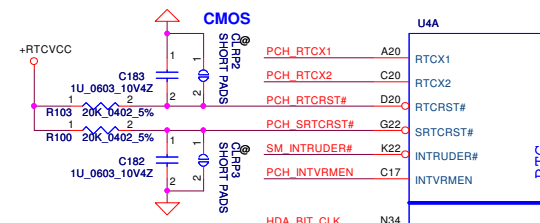
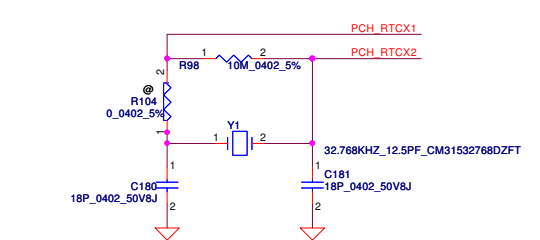
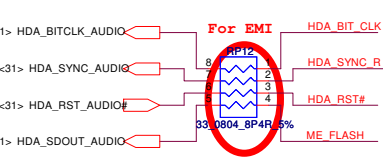
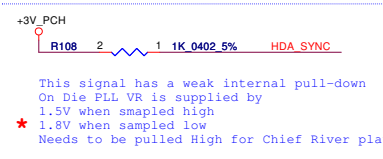
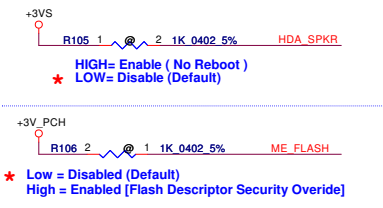
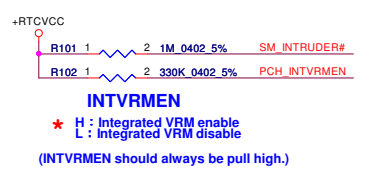
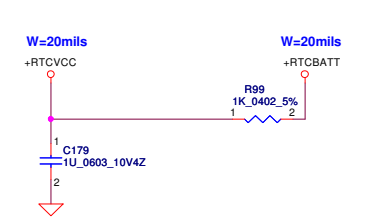


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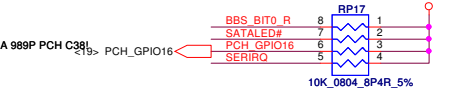
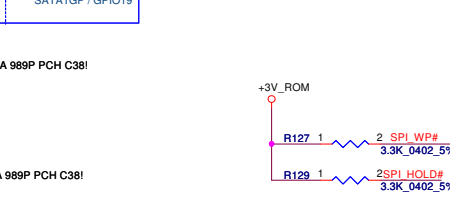
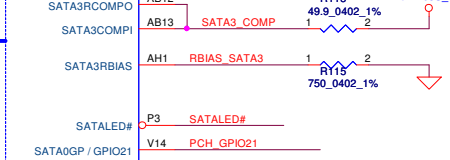
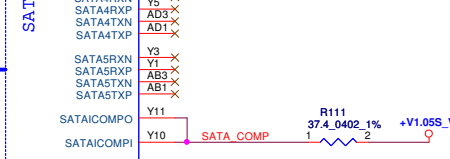
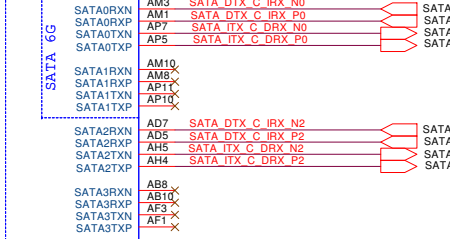
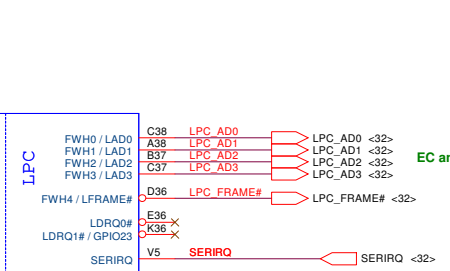






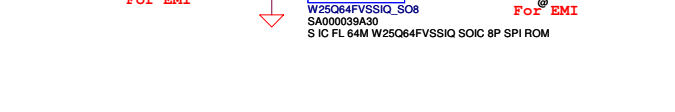
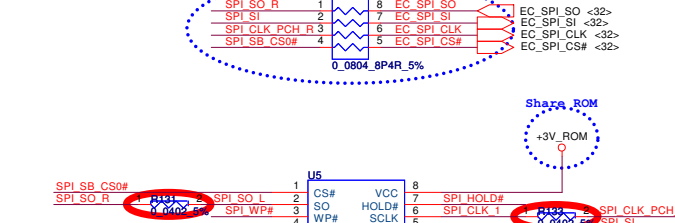
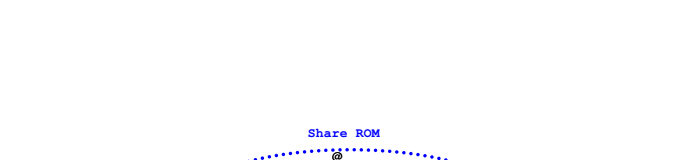
CLR2	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

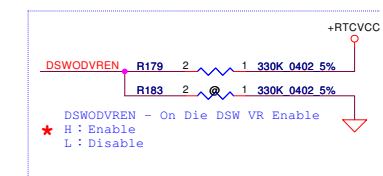
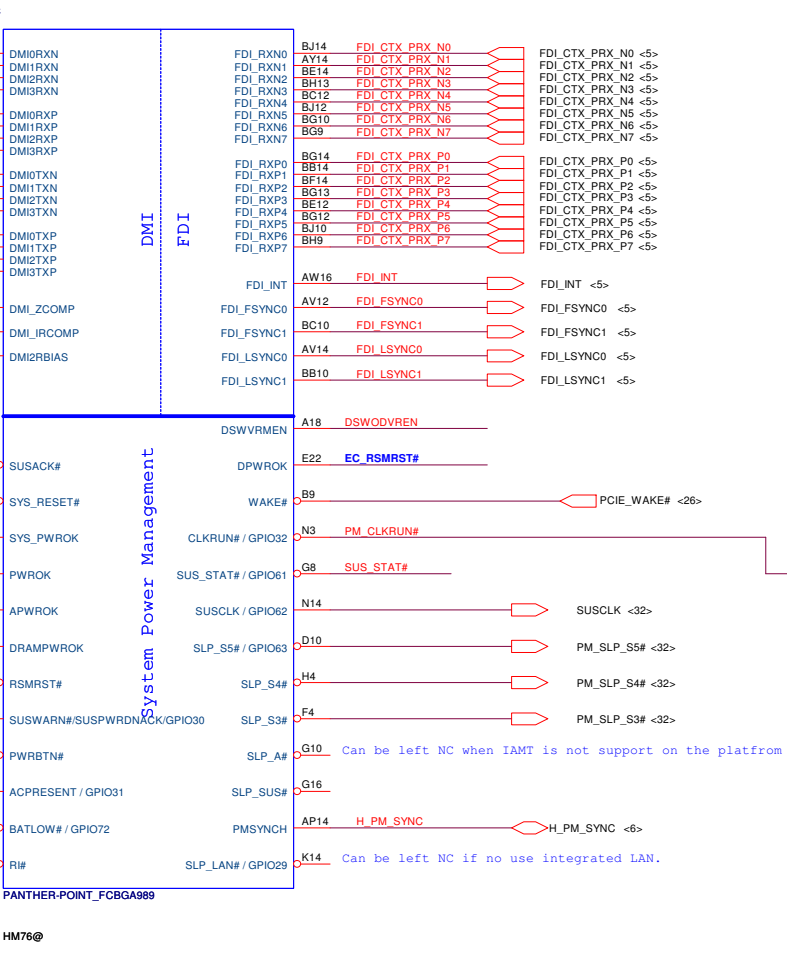
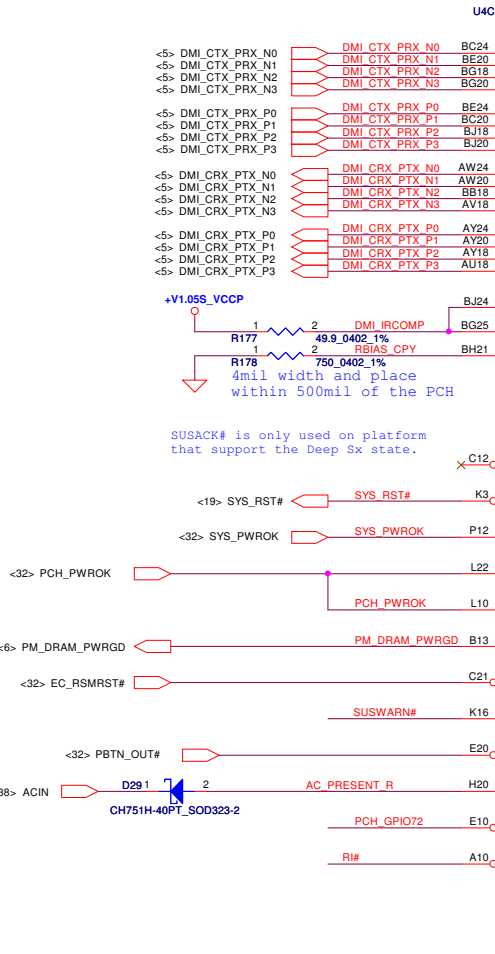
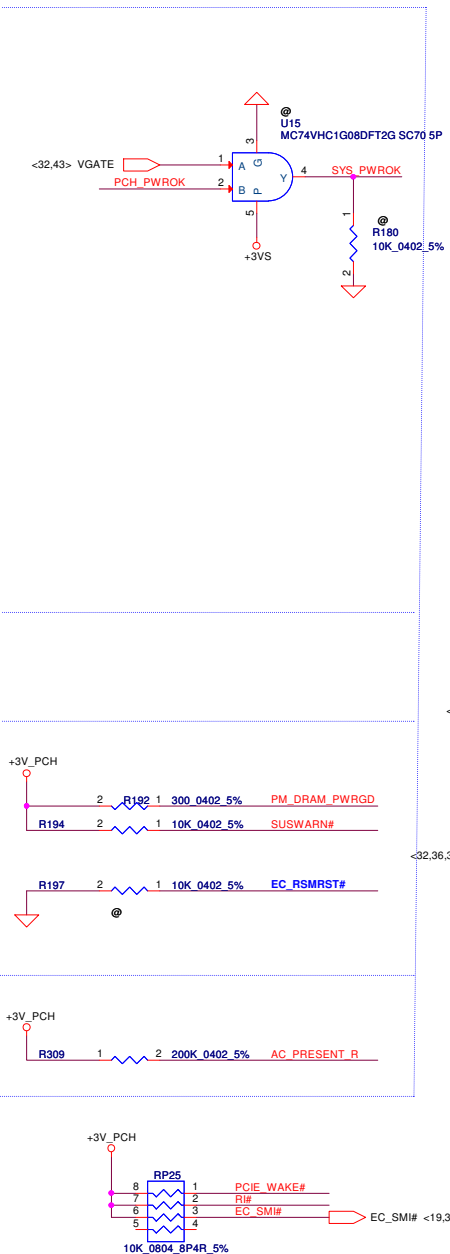
CLR3	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers



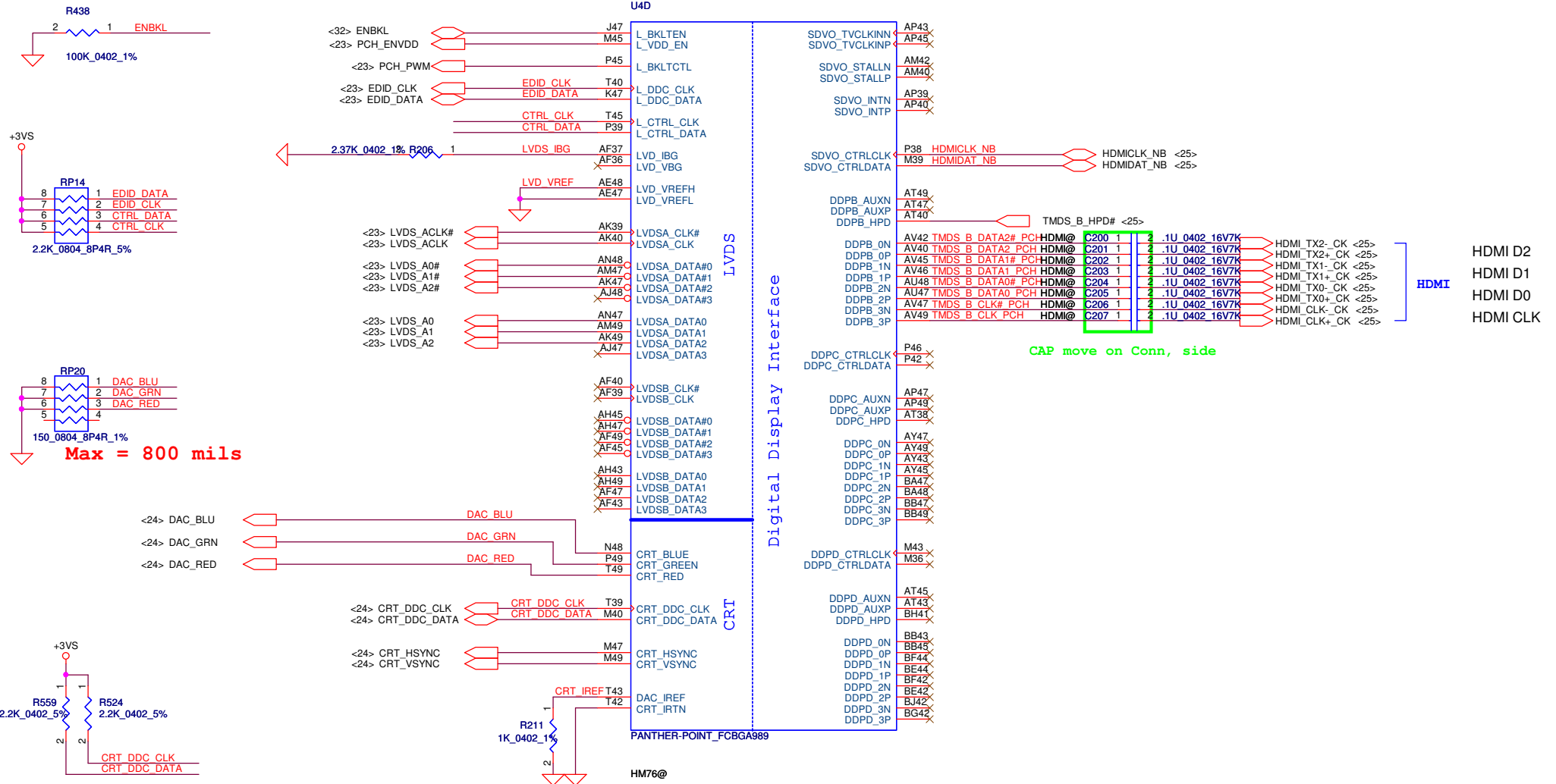
CLR2	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

CLR3	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

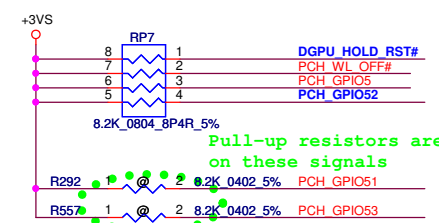
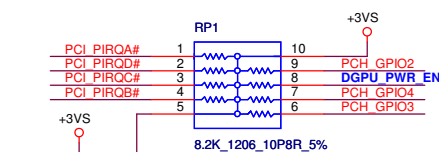




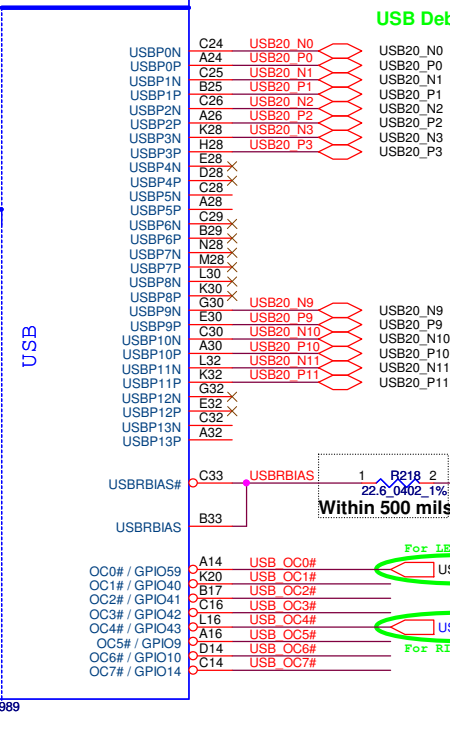
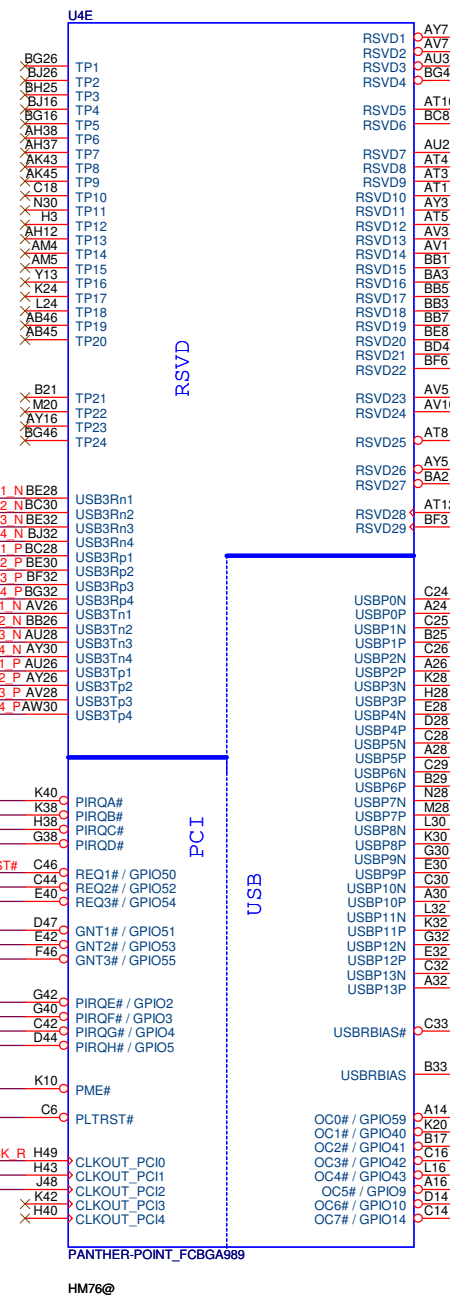
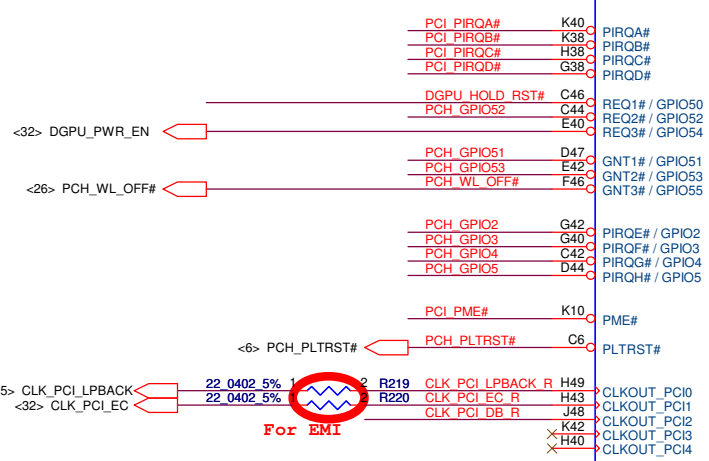
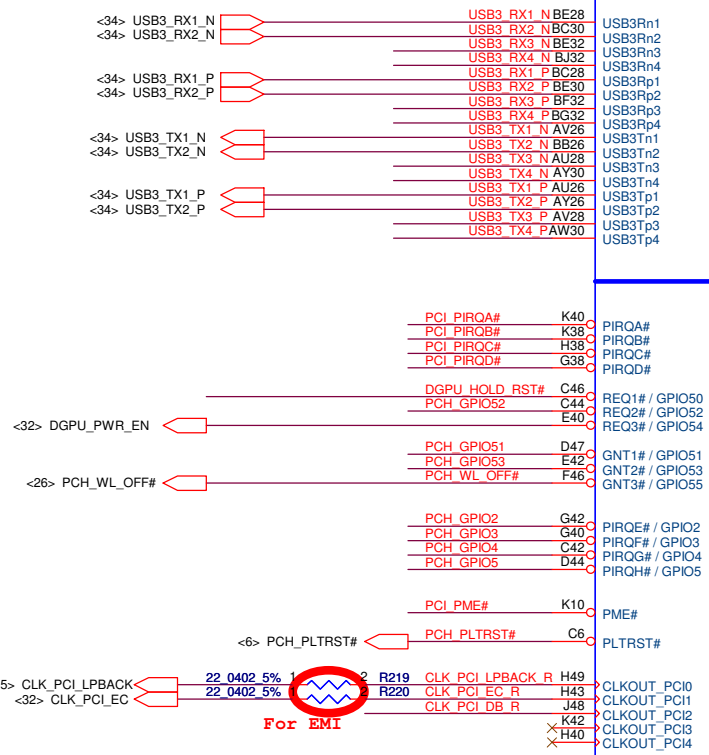
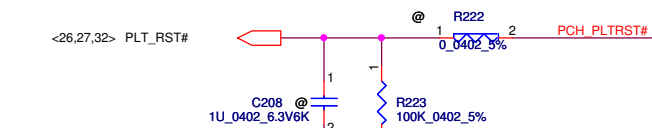
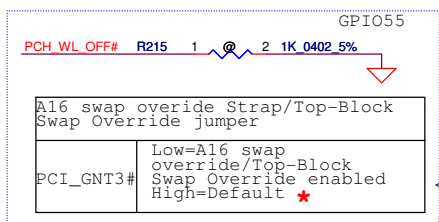
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Issued Date	2011/06/15	Deciphered Date	2012/07/11	PCH (3/9) DMI,FDI,PM,	
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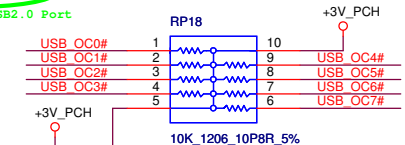
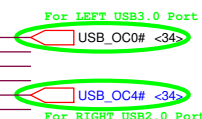
Boot BIOS Strap bit1 BBS1			
	Bit11	Bit10	Destination
GNT1# / GPIO51	0	1	Reserved
	1	0	Reserved
	1	1	★ SPI (Default)
	0	0	LPC



USB Debug Port = Port1 and Port9

LEFT USB (USB 3.0)
LEFT USB
Touch Screen
USB Camera

RIGHT USB
WLAN
CARD READER



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The schematic diagram illustrates the connection between the Mars XT and Sun Pro boards. Both boards are connected to a common PCH_GPIO71 signal line. The Mars XT board (left) features a PCH_GPIO65 signal and a Mars XT label. The Sun Pro board (right) features a PCH_GPIO71 signal and a Sun Pro label. A table in the center shows the PCH_GPIO71 signal mapping: 1 for Mars XT and 0 for Sun Pro. The boards are connected to a +3VS power source and a 10K_0402_5% resistor network.

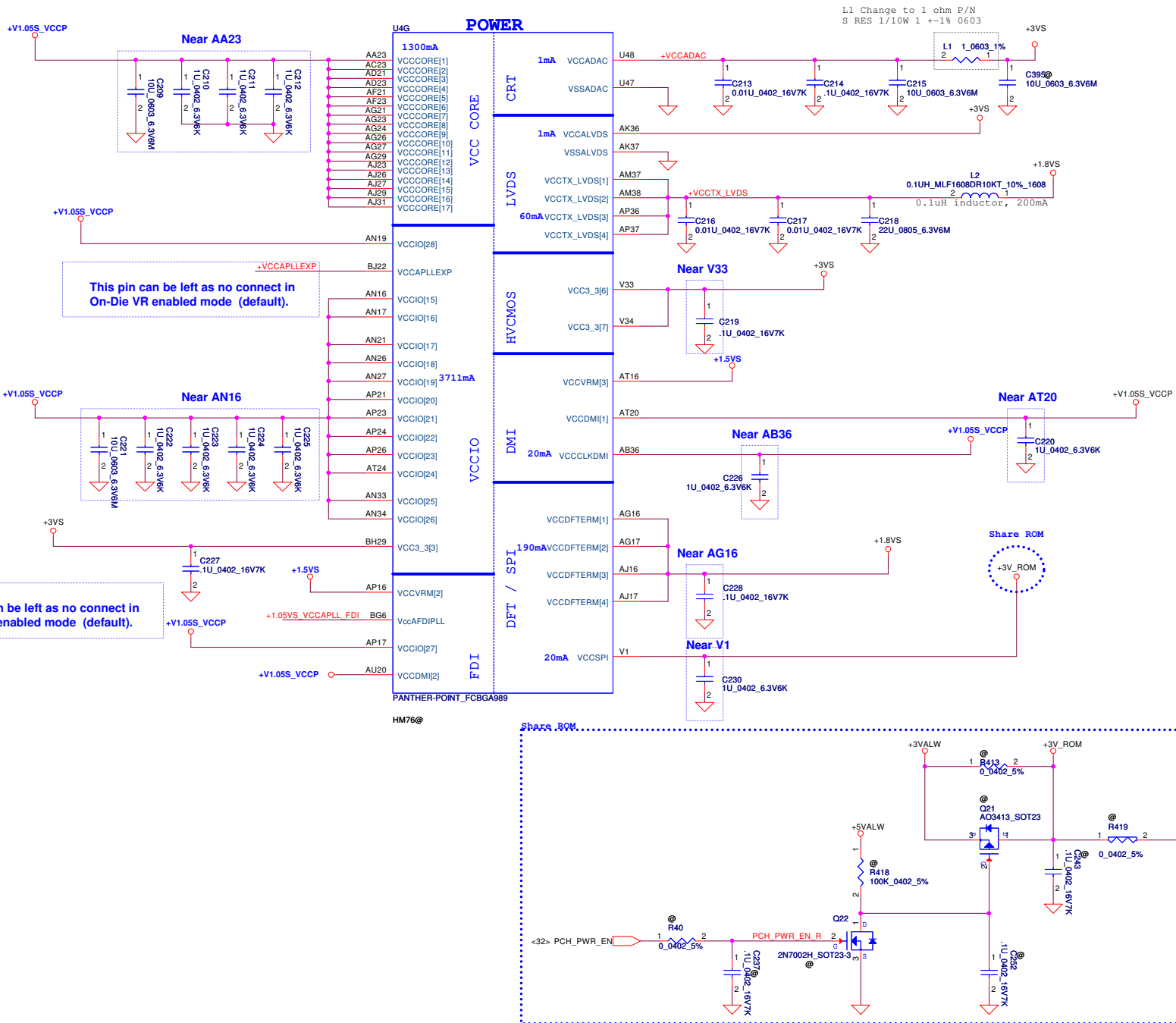
PCH_GPIO71	Function
1	Mars XT
0	Sun Pro

R240 1 2 1K_0402_5% PCH_GPIO28

R245 1 @ 2 10K_0402_5% PCH_GPIO27

0	0	SG(Optimus / PX)

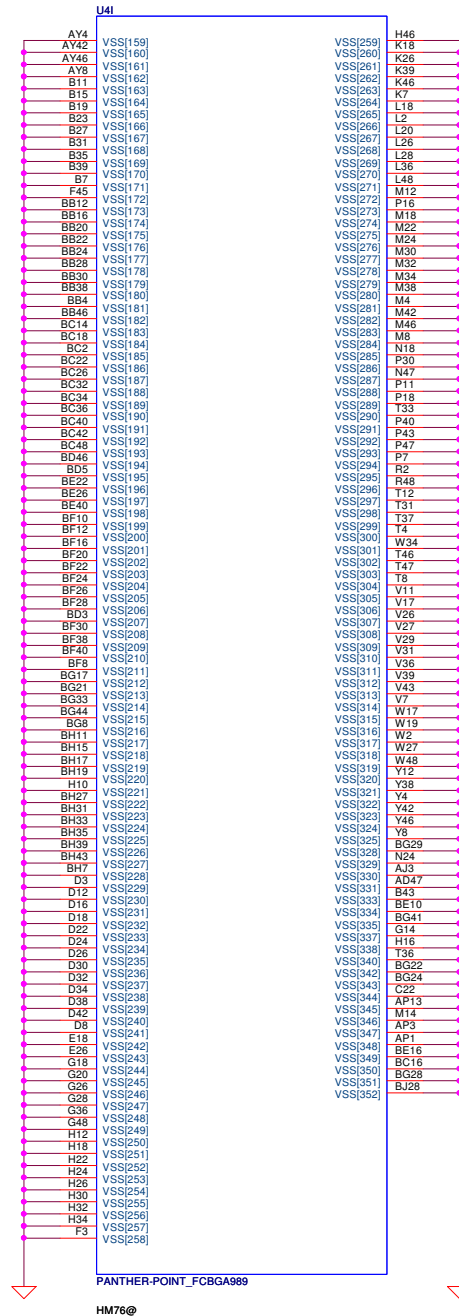
Security Classification	Compal Secret Data			Title	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Size	Rev
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				Custom	
				Date:	Wednesday, February 27, 2013
				Sheet	19 of 60



On-Die PLL Voltage Regulator
H: On-Die PLL voltage regulator enable
VCCFDIPLL, VCCAPLLEXP, VCCAPLLDMI2, VCCAPLLSATA

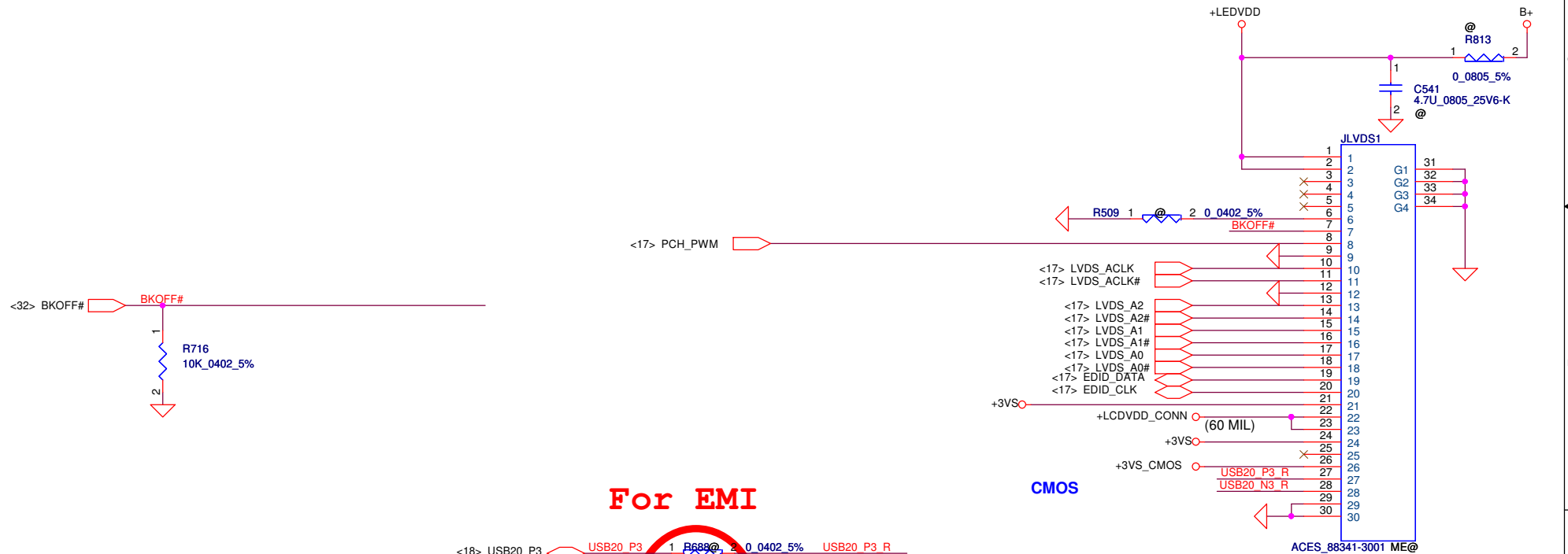
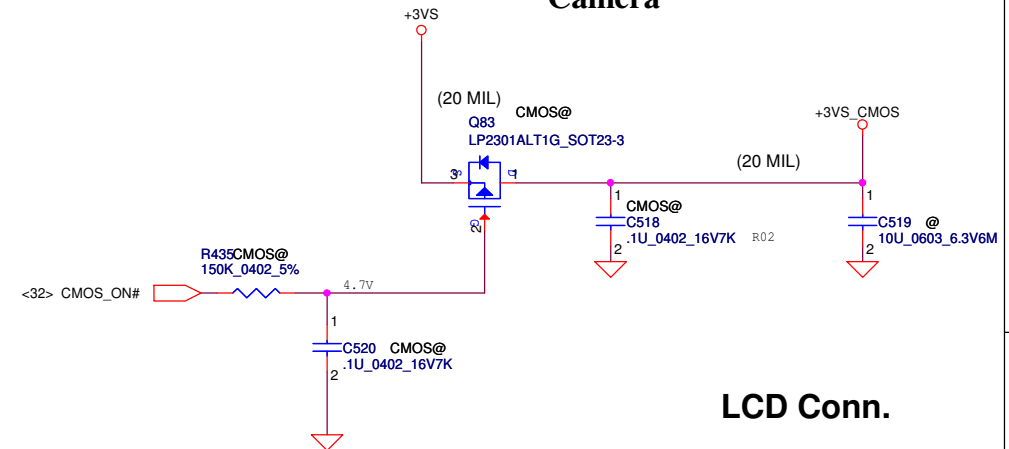
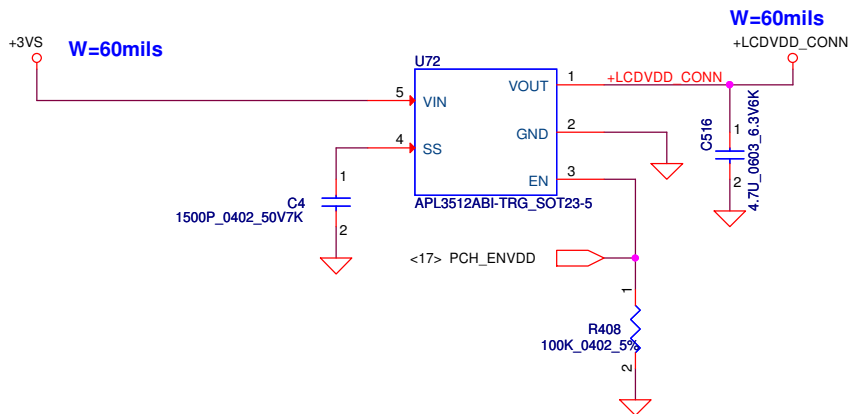
On-Die PLL Voltage Regulator
H: On-Die PLL voltage regulator enable
VCCFDIPLL, VCCAPLLEXP, VCCAPLLDMI2, VCCAPLLSATA

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				Date	Wednesday, February 27, 2013
				Sheet	21 of 60

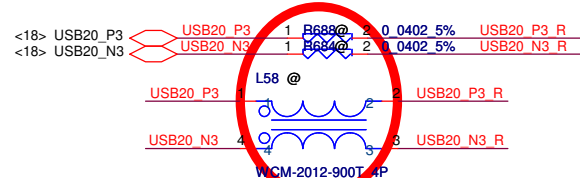


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				Custom LA-9632P	
Date:	Wednesday, February 27, 2013	ISheet	22	of	60

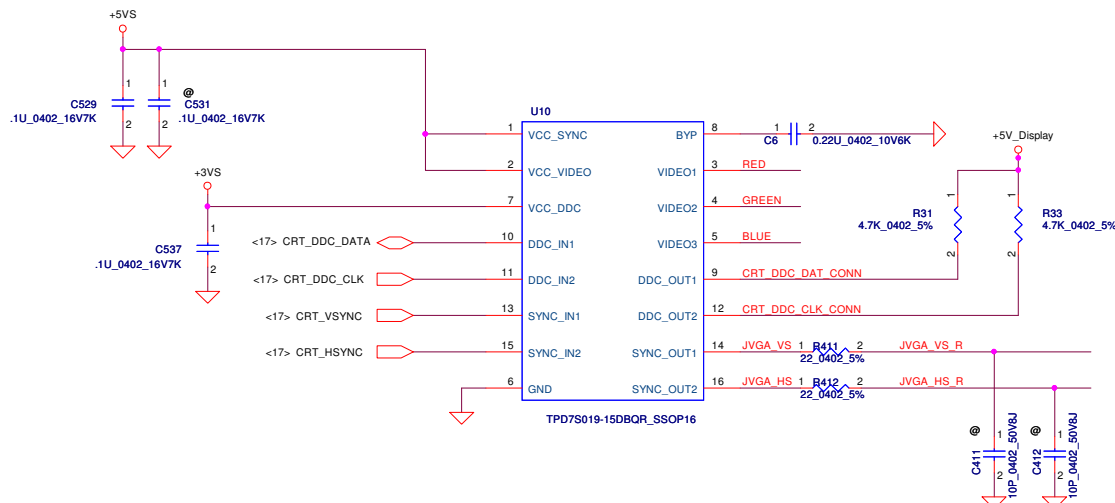
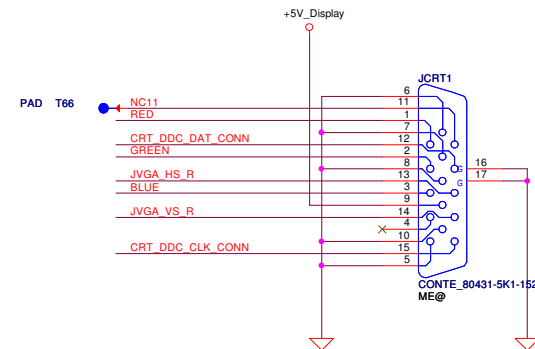
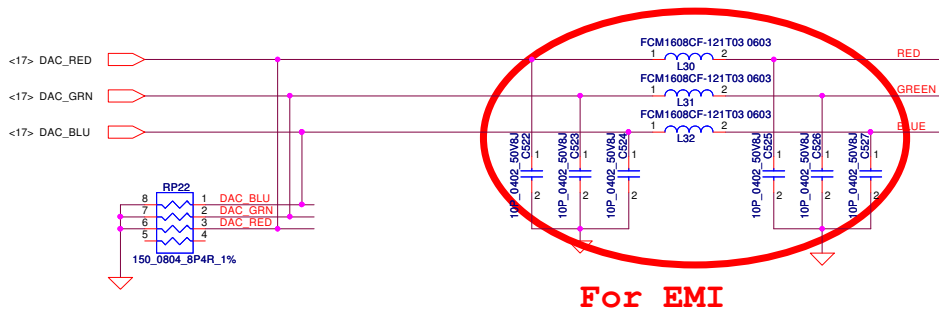
LCD POWER CIRCUIT



For EMI

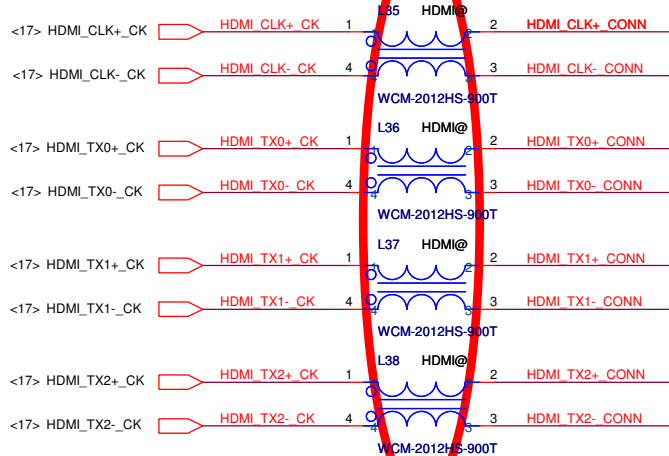


Security Classification		Compal Secret Data				Compal Electronics, Inc.									
Issued Date		2011/06/15		Deciphered Date		2012/07/11		Title							
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								Size Custom	Document Number LA-9632P						Rev 1.0
								Date:		Wednesday, February 27, 2013				Sheet 23 of 60	

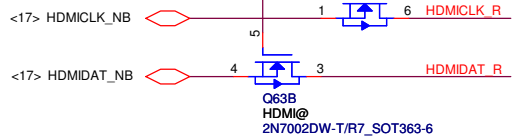
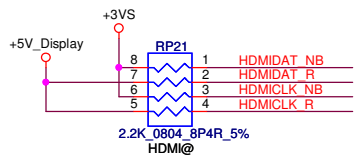


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				Custom	1.0
				Date	Wednesday, February 27, 2013
				Sheet	24 of 60

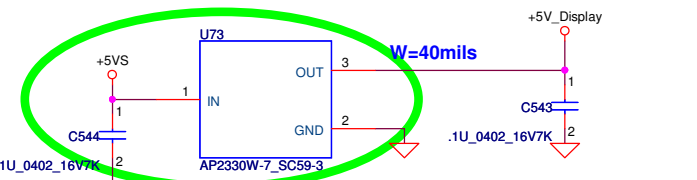
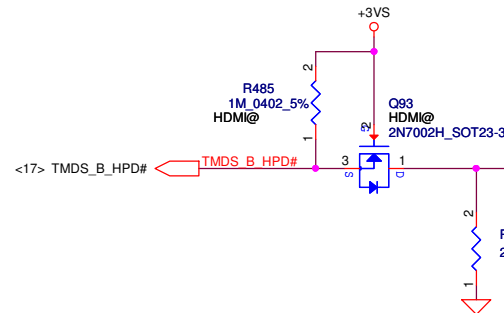
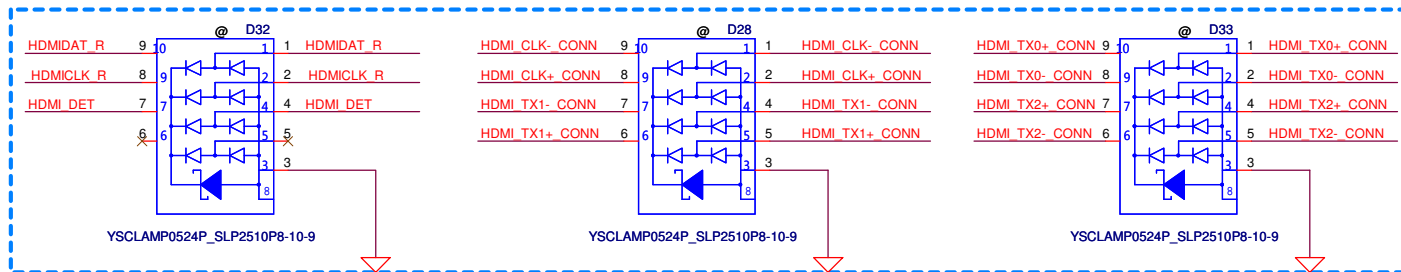
For EMI



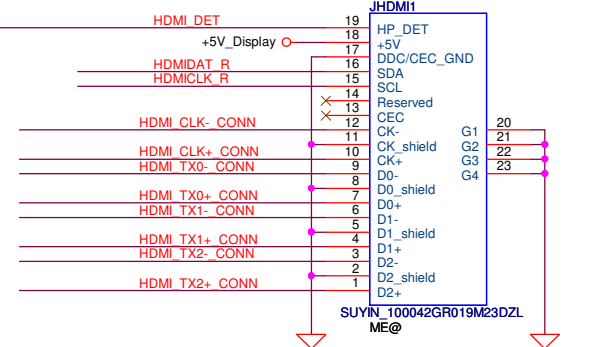
Pull up R for PCH OR VGA SIDE



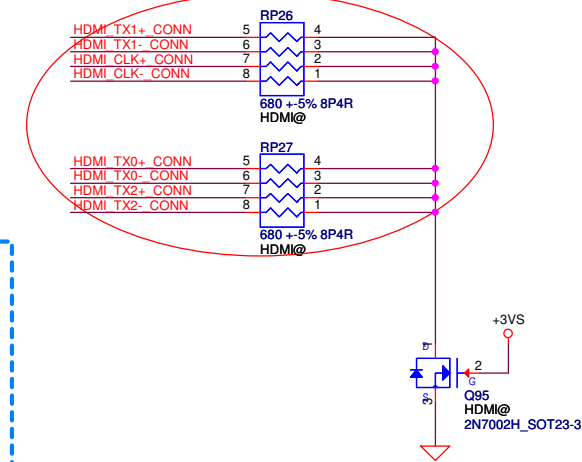
ESD



For CRT and HDMI

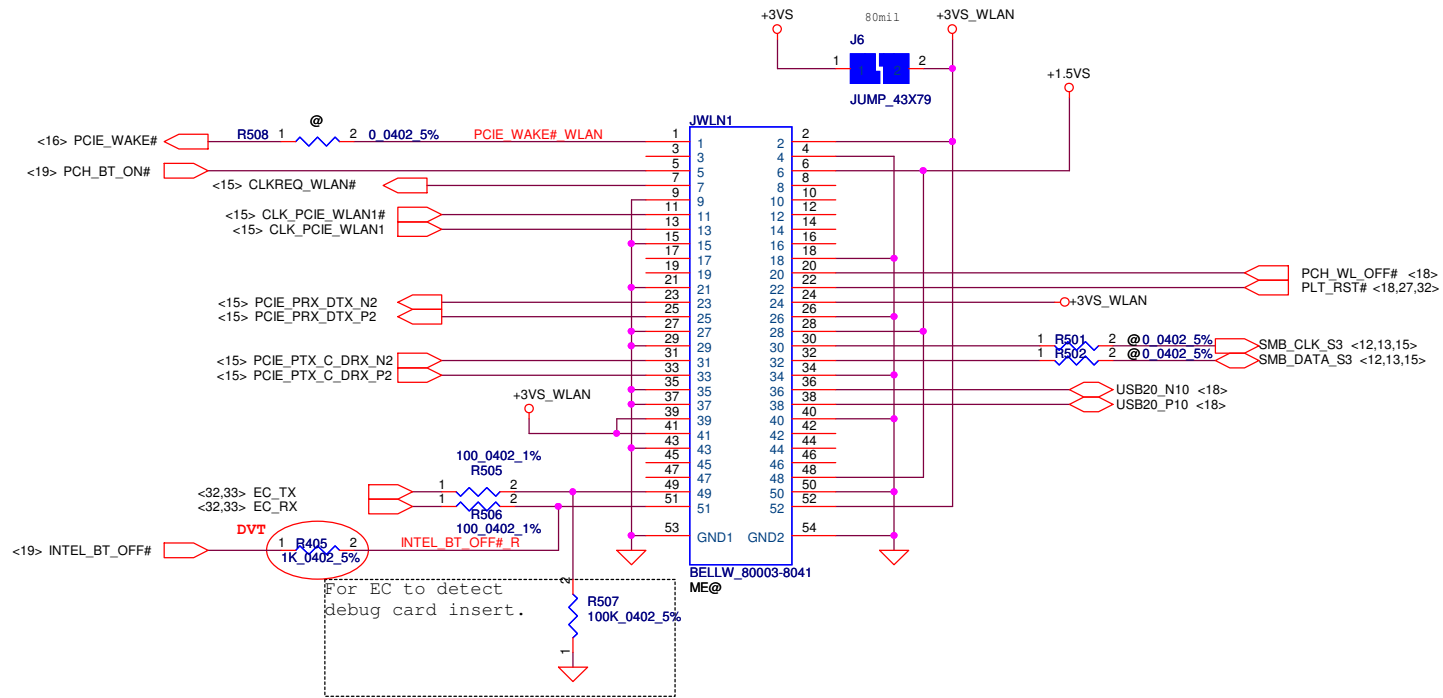


DVT



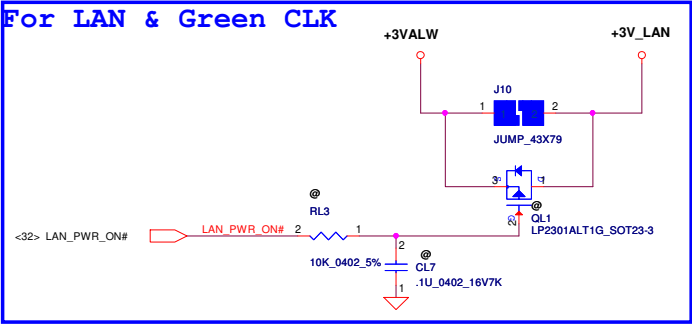
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	HDMI CONN
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				LA-9632P	Rev 1.0
				Date: Wednesday, February 27, 2013	Sheet 25 of 60

Mini Card for WLAN/WiMAX(Half)

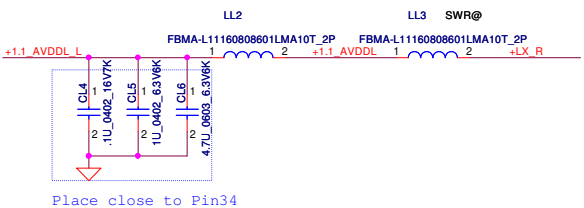
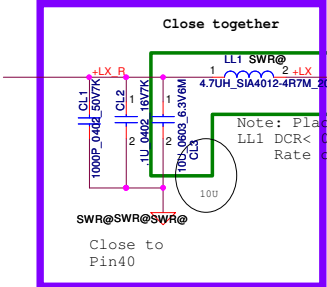
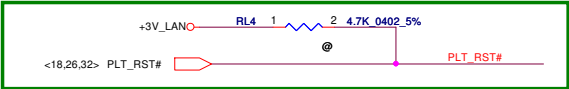


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					LA-9632P
				Date:	Wednesday, February 27, 2013
				Sheet	26 of 60
				Rev	1.0

For LAN & Green CLK

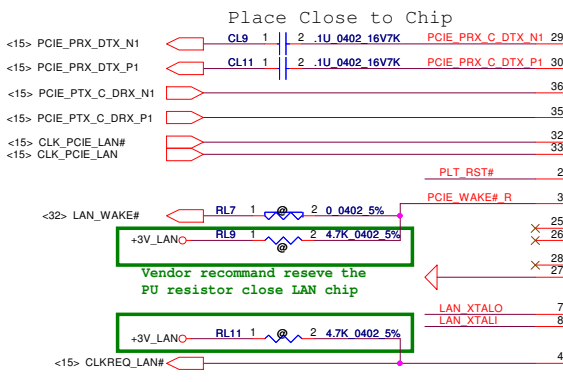


Vendor recommend reseve the
PU resistor close LAN chip

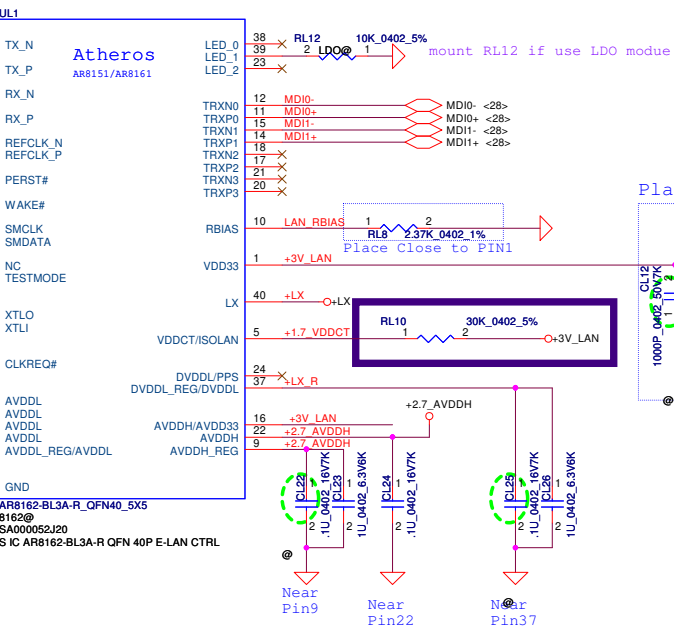
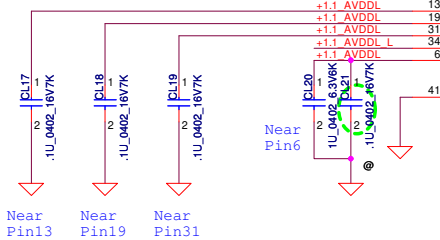


Place close to Pin34

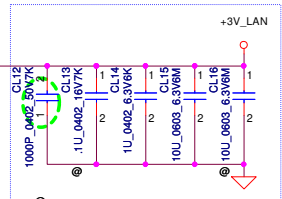
UL1 8172@
QCA8172-BL3A-R
SA00005410
S IC QCA8172-BL3A-R QFN 40P E-LAN CTRL



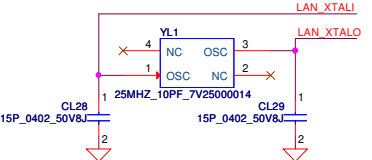
Vendor recommend reseve the
PU resistor close LAN chip



Place Close to PIN1



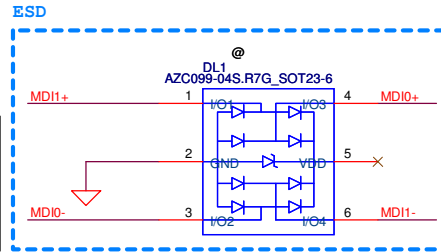
don't @ (could be B C cost done)



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				Date	Wednesday, February 27, 2013
				Sheet	27 of 60

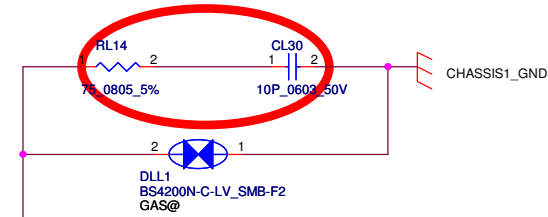
DL1
1'S PN:SC300001G00
2'S PN:SC300002E00

Place Close to TL1



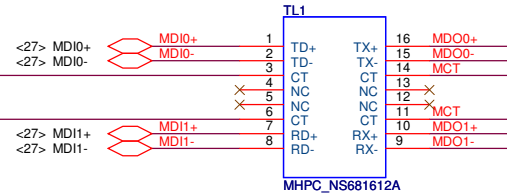
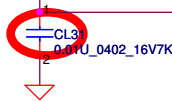
Reserve gas tube for EMI go rural solution

For EMI

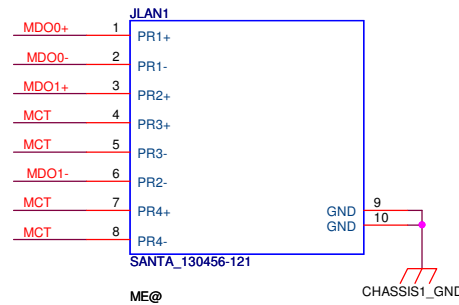
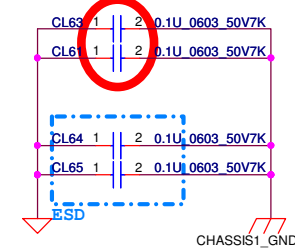


Place Close to TL1

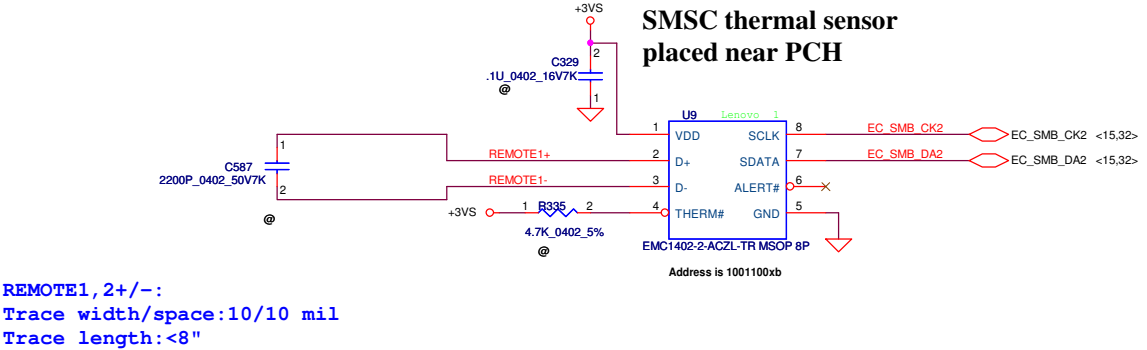
For EMI



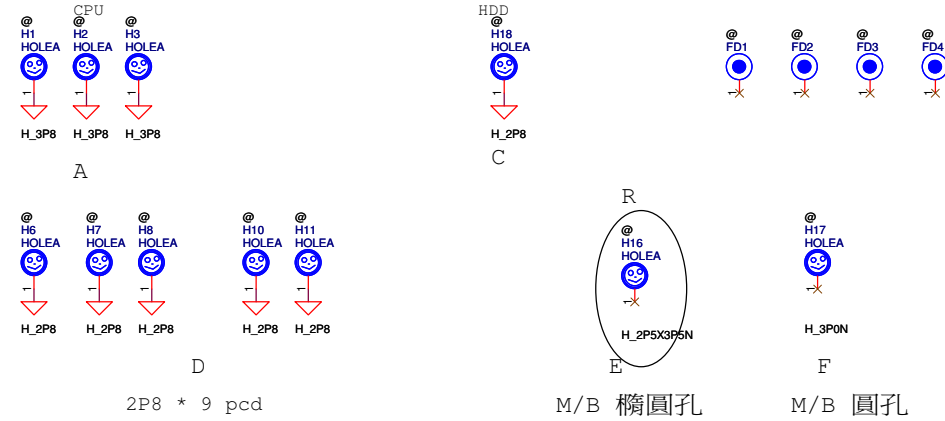
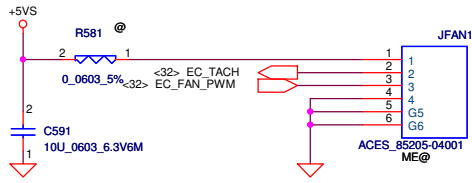
For EMI



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					LA-9632P
				Date:	Wednesday, February 27, 2013
				Sheet	28 of 60
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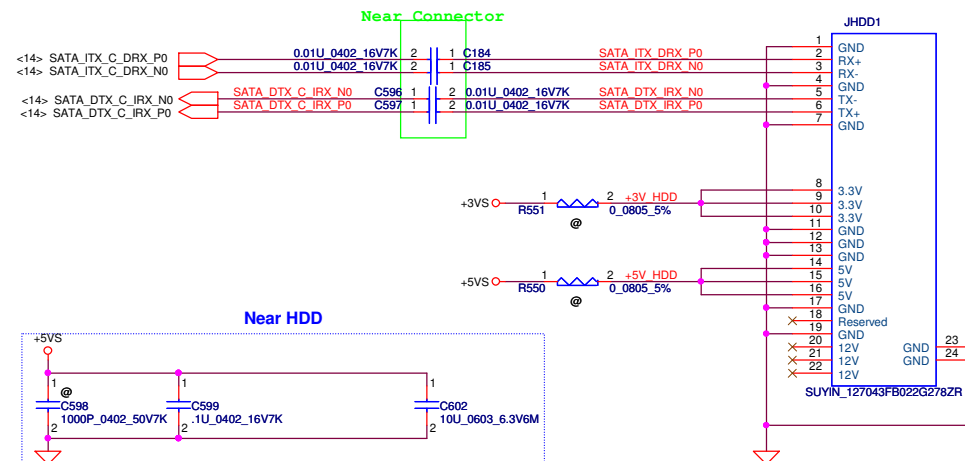


FAN1 Conn

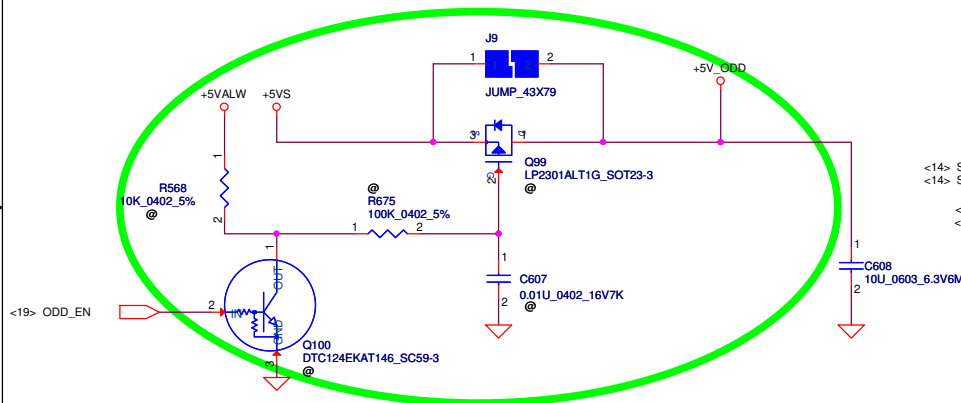


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				Date: Wednesday, February 27, 2013	Sheet 29 of 60

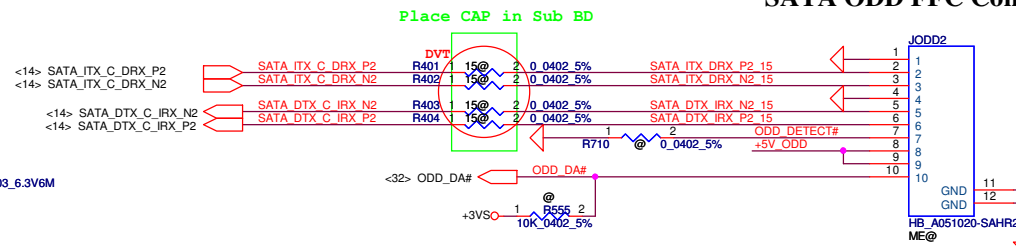
SATA HDD Conn.



ODD Power Control

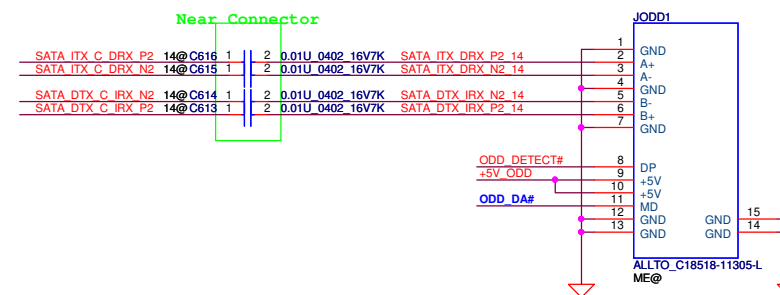


FOR 15" SATA ODD FFC Conn.



Co-lay

FOR 14" SATA ODD Conn.

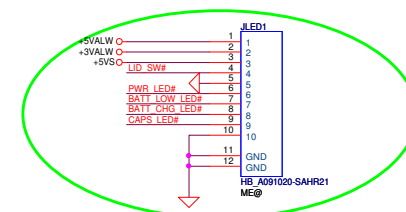
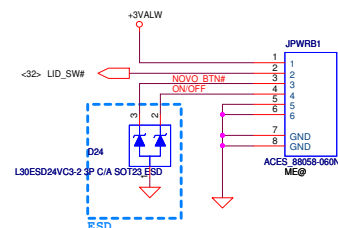
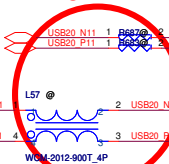
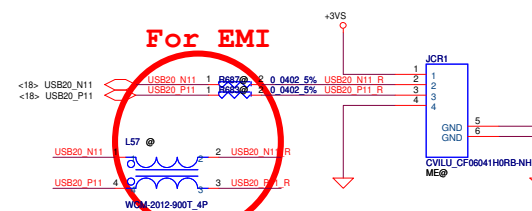
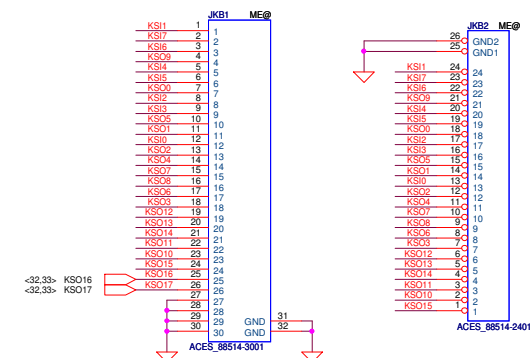
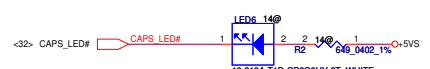
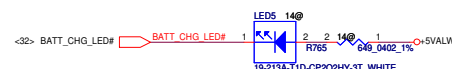
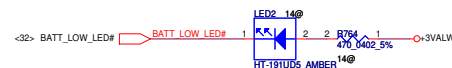
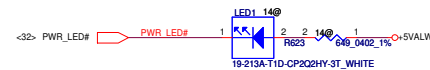
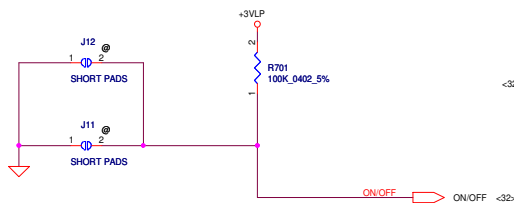


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				Size	Rev
				Custom	1.0
				LA-9632P	
				Date	Wednesday, February 27, 2013
				Sheet	30 of 60

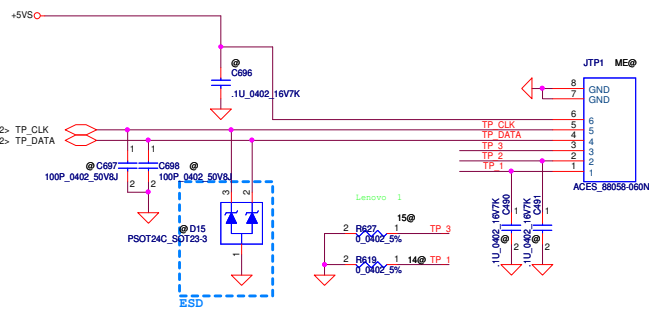
An integrated 3.3 V to 1.8V Low-dropout voltage regulator (LDO).



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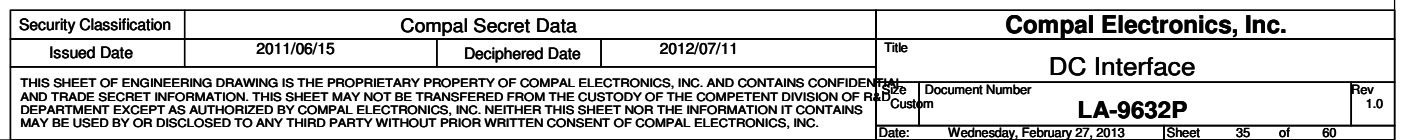
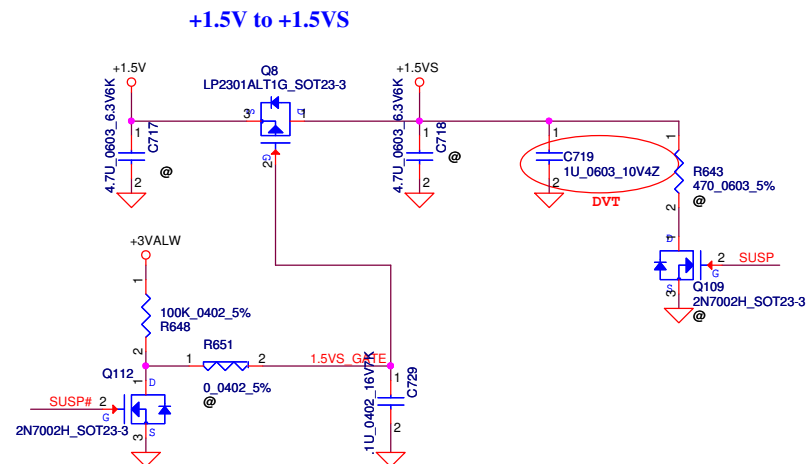
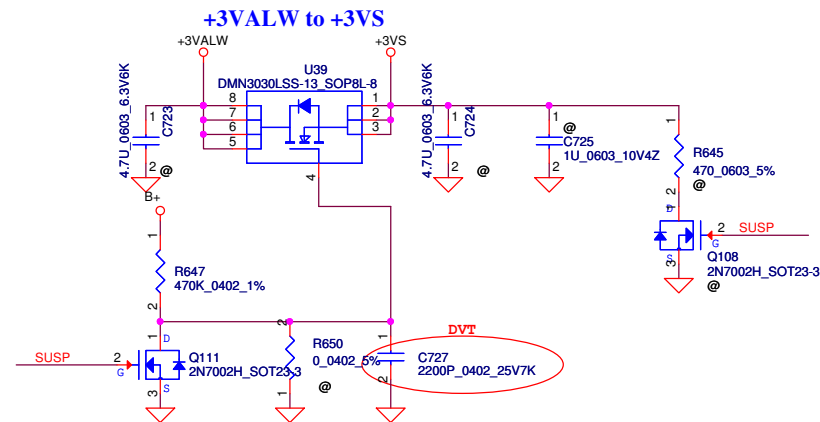


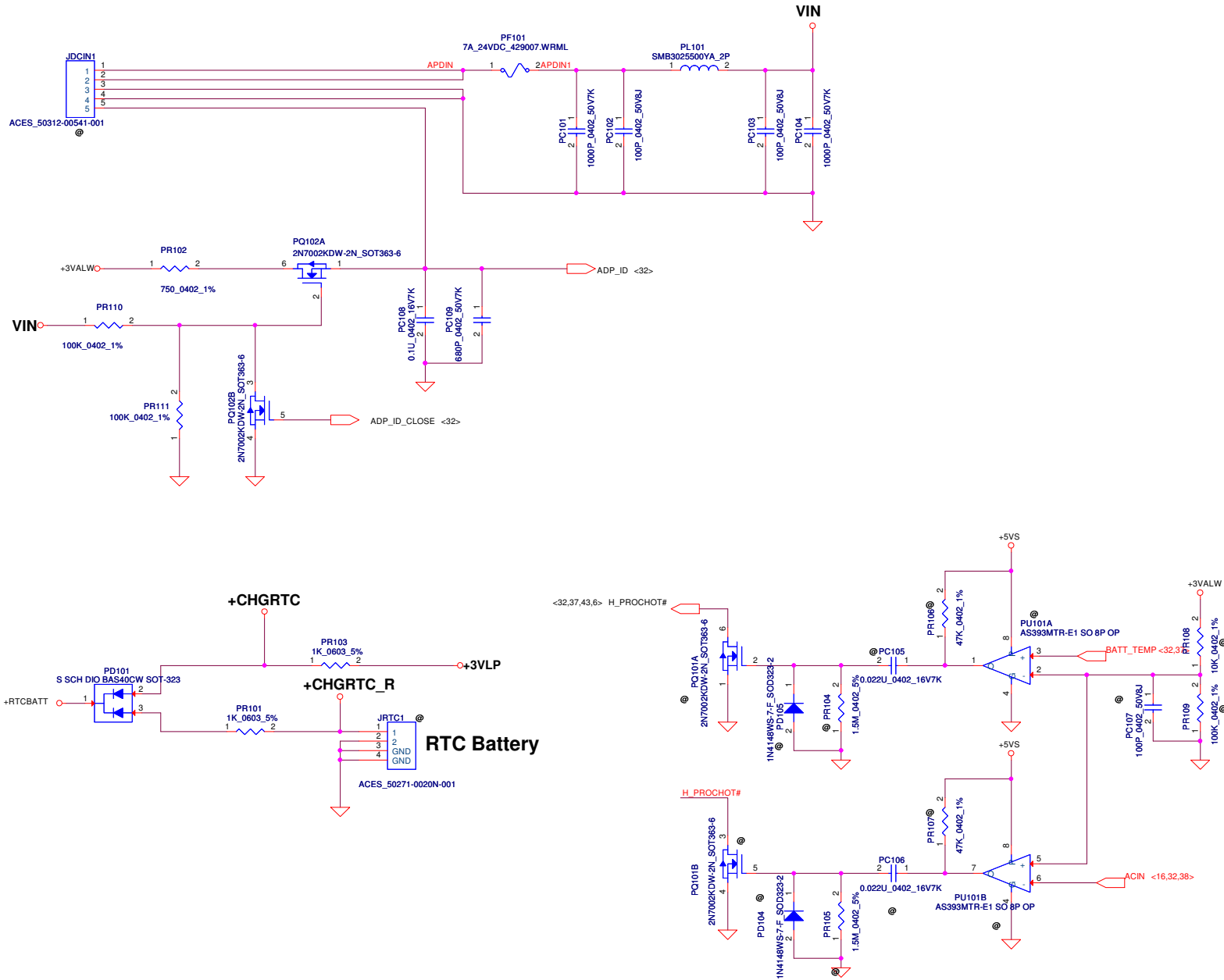
For 15"



15/17"	
1	VCC
2	CLK
3	DAT
4	GND
5	L
6	R

14"	
1	VCC
2	CLK
3	DAT
4	L
5	R
6	GND

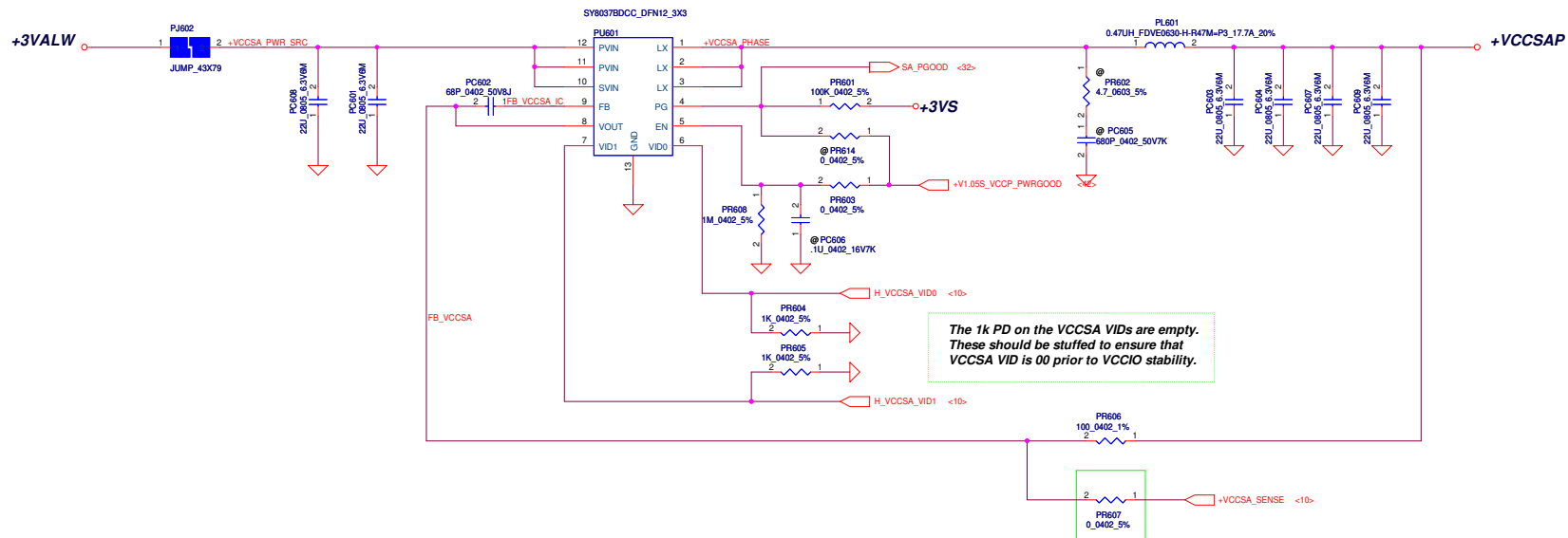
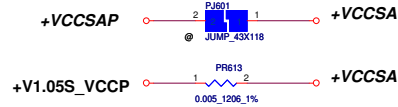




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				Date	Wednesday, February 27, 2013
				Sheet	36 of 60
				Rev	1.0

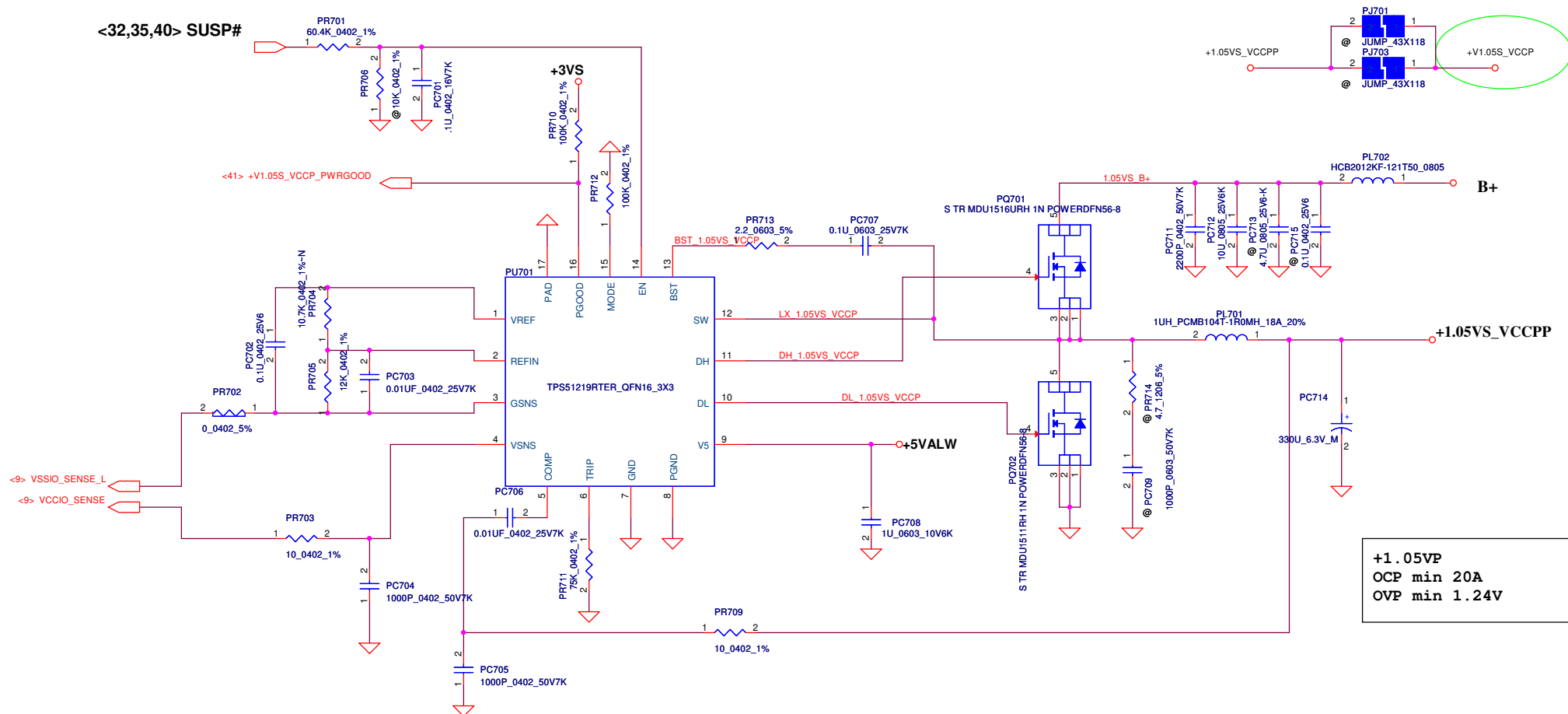
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

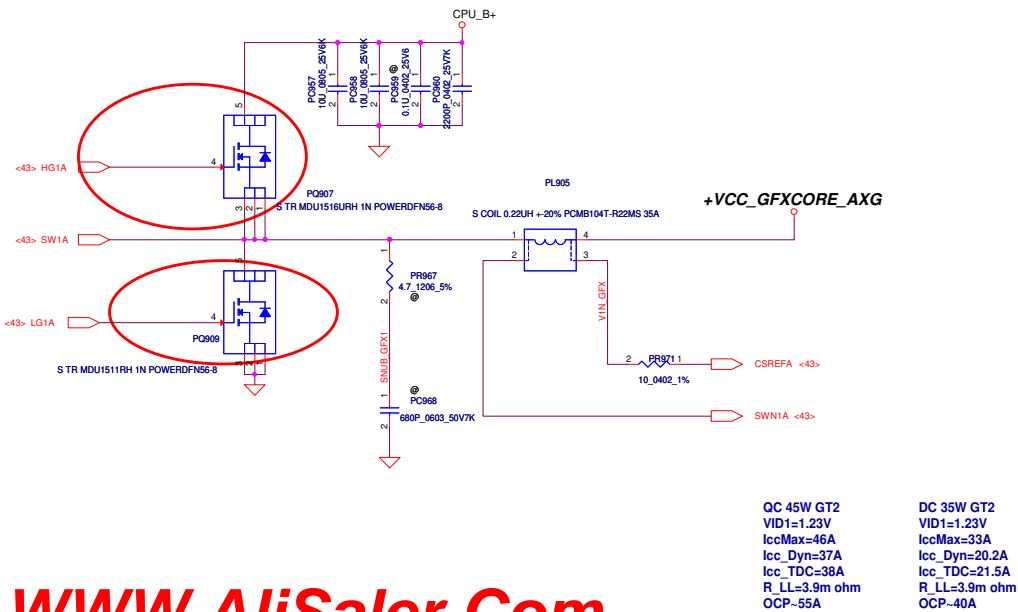
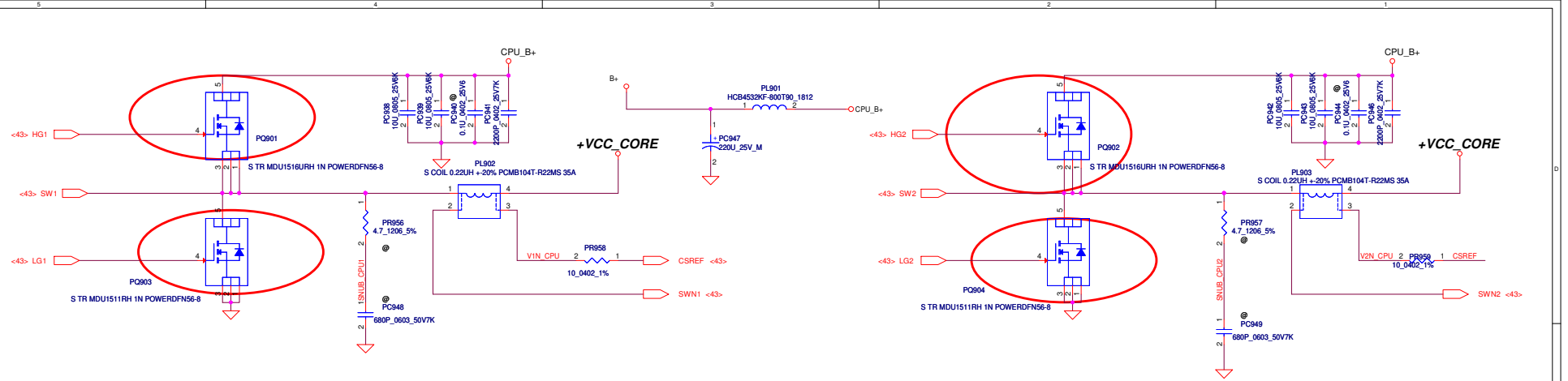


The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

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				Document Number
				Gx00-CR
				Rev
				1.0
				Date: Wednesday, February 27, 2013
				Sheet 41 of 60

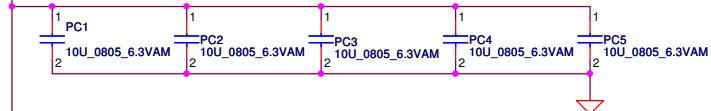


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				Date	Wednesday, February 27, 2013
				Sheet	42 of 60
				Rev	1.0

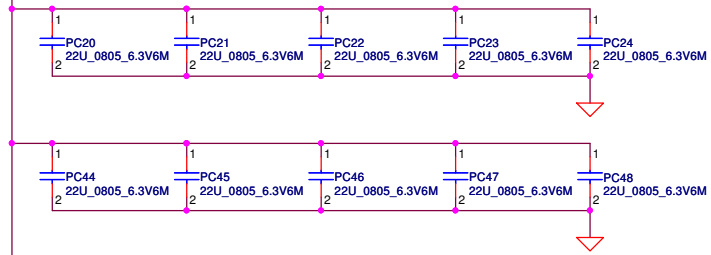


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Size	Document Number	Gx00-CR		Rev	
D		1.0		Date	
Wednesday, February 27, 2013		Sheet		44 of 60	

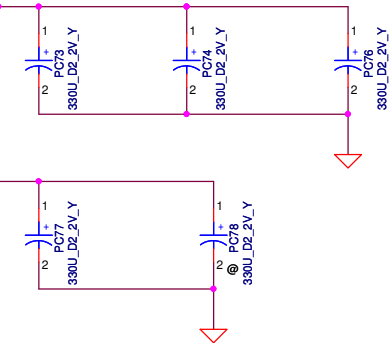
+VCC_CORE



+VCC_CORE



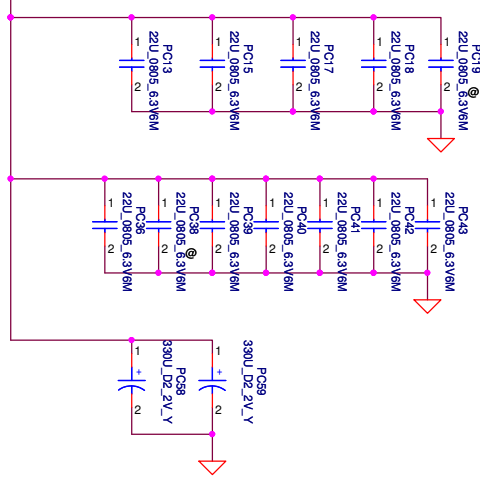
+VCC_CORE



+VCC_CORE

+VCC_GFXCORE_AXG

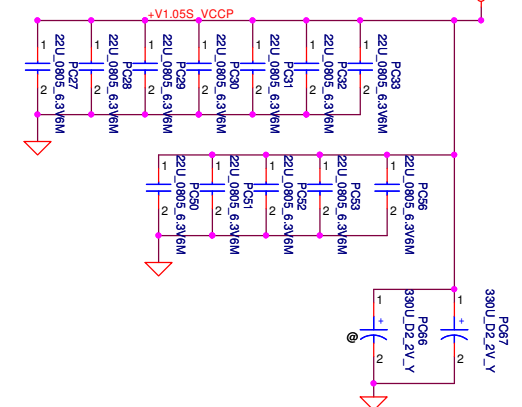
+VCC_GFXCORE_AXG



Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites

+V1.05S_VCCP

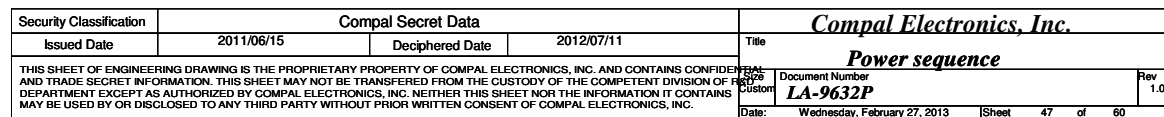


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Date: Wednesday, February 27, 2013				Sheet 45	of 60

VIWGP/R HW PIR List

Item	Page	MODIFICATION LIST	PURPOSE	EVT TO DVT
1	P. 46	Add PR102, PC108, PC109	For ADP_ID pin detect	
2	P. 47	Add PR225, PR227, PR228, PQ206, PQ207, PQ208	For protect adapter function	
3	P. 49	Add PR410, PC433	For 3VALWP/5VALWP sequence	
4	P. 49	Add PC434, PC435, PC436, PC437	For EMI solution	
5	P. 49	Add PC432 and change PL404 from 1.5uH to 3.3uH	For improve output voltage ripple	
6	P. 50	Change PR502 from 49.9k to 64.9k	For +0.75VSP sequence	
7	P. 51	Add PC637	For +0.95VGSP sequence	
8	P. 54	Change PC907, PR912, PR927, PC928	For CPU Transient Compensation	
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23				
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25				

MODEL NAME: *Power Sequence Block Diagram*
PCB NAME: *LA-9631P*
REVISION:
DATE: *2011/07/13*



VIWGP/R HW PIR List

Item	Page	MODIFICATION LIST	PURPOSE	EVT TO DVT
1	P. 36	Change C726, C727 to 2.2nF	For Sequence	
2	P. 26	Add R405	For Intel Combo Card	
3	P. 25	Delete RP19. Add RP26, RP27	Because ME modify MIC location	
4	P. 14	Add R406, R407, R408, R409	Reserve for improvement factory processes	
5	P. 32	Add EC_SPI_S0, EC_SPI_S1, EC_SPI_CLK, EC_SPI_CS# to EC	Reserve for improvement factory processes	
6	P. 32	Add PCH_PWR_EN to EC Pin.107	Reserve for improvement factory processes	
7	P. 32	Reserve R410	Reserve Pull-high for GPIO	
8	P. 5~22	Change footprint of JCPU1, U4	For Lenovo rule	
9	P. 21	Add Q21, R40, C237, R225, C243	Reserve for power consumption	
10	P. 24	Add R411, R412, C411, C412	Reserve for EMI	
11	P. 32	Add ADP_65 to EC Pin. 21	For adapter protection	
12	P. 32	Add ADP_90 to EC Pin. 68	For adapter protection	
13	P. 32	Add ADP_135 to EC Pin. 85	For adapter protection	
14	P. 32	Change EC_FAN_PWM from EC Pin. 34 to EC Pin. 26	For common design	
15	P. 32	Change NOVO# from EC Pin. 26 to EC Pin. 34	For common design	
16	P. 32	Add ADP_ID to EC Pin. 66	For adapter	
17	P. 32	Change PCH_ENBKL from EC Pin. 73 to EC Pin. 76	For common design	
18	P. 32	Change IMVP_IMON from EC Pin. 76 to EC Pin. 73	For common design	
19	P. 32	Add VGATE to EC Pin. 74	Reserve for sequence	
20	P. 32	Add SYS_PWROK to EC Pin. 86	Reserve for sequence	
21	P. 32	Change EC_TS_ON# from EC Pin. 85 to EC Pin. 97	For common design	
22	P. 32	Change DGPU_PWR_EN from EC Pin. 107 to EC Pin. 123	For common design	
23	P. 32	Change SUSCLK from EC Pin. 123 to EC Pin. 122	For common design	

VIWGP/R HW PIR List

Item	Page	MODIFICATION LIST	PURPOSE	
1	P. 30	Delete R416, Add J9	No need Zero ODD Function	. DVT TO PVT
2	P. 26	Reserve R508	For leakage current issue of Atheros WLAN	
3	P. 23	Add R509	protect BKOFF# damage	
4	P. 32	Reserve R416	Reserve +3VLP power rail to EC	
5	P. 32	Change EC_RST# power rail to +3V_EC	Using power rail which the same with EC.	
6	P. 32	Change EC_SMB_CK1 & EC_SMB_DA1 power rail to +3V_EC	Using power rail which the same with EC.	
7	P. 14	Change U5 from 4MB to 8MB ROM	Follow common design	
8	P. 14	Delete R266, R221, U6	It is for 2MB ROM, we don't need it	
1	P. 31	Reserve resistance to +3VLP and +3VALW.	For Speaker Noise in S5	
2	P. 32	Reserve resistance in EC for share ROM.	Follow common design	
3	P. 41	Reserve +V1.05S_VCCP_PWRGOOD of +V.05S_VCCP to connect to SA_PGOOD	For Celeron CPU	